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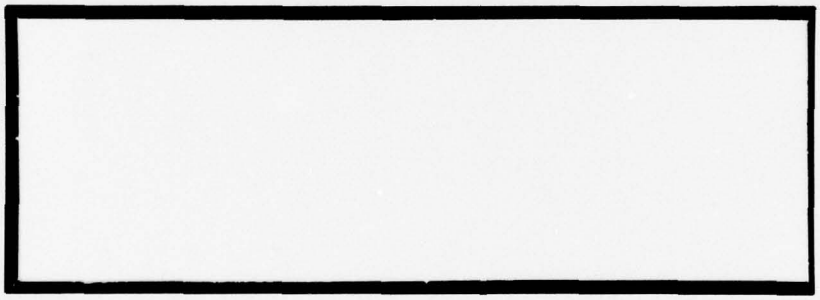


ELECTRICAL ENGINEERING

ENGINEERING EXPERIMENT STATION
AUBURN UNIVERSITY
AUBURN, ALABAMA

FINAL TECHNICAL REPORT

Contract DAAH01-76-C-0328

B. D. Carroll, K. B. Cook, Jr., G. R. Kane

H. T. Nagle, Jr., and T. D. Slagh

Co-Project Leaders

December, 1976

Prepared for

U. S. Army Missile Command

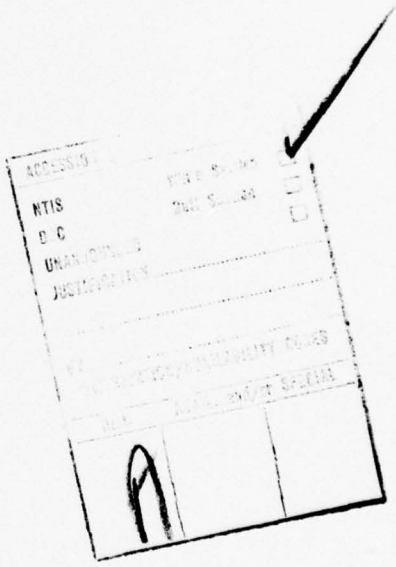
Redstone Arsenal, Alabama

Prepared by

Electrical Engineering Department
Auburn University
Auburn, Alabama

FOREWORD

This final technical report is submitted to the U.S. Army Missile Command by the Electrical Engineering Department, Auburn University, to complete its contract obligations under contract DAAH01-76-C-0328. This report is published in nine parts, each separate and independent of the others. Each part summarizes significant work related to the contract tasks completed during the period of contract performance.



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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report investigates the problems involved in implementing hybrid integrated circuits. Its nine separte parts address hybrid integration, computer-aided thermal modeling, thermal simulation, thermal analysis and measurement, thick film resistor noise, noise in optical isolators, automated conductor routing, interactive schematic generation, and computer aided design.

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FINAL REPORT CONTENTS

Part 1

THE HYBRID INTEGRATION OF A MULTISTAGE ACTIVE BANDPASS FILTER/AMPLIFIER

K. B. Cook, Jr., D. V. Kerns, Jr., H. T. Nagle, Jr.,
T. D. Slagh, and V. W. Ruwe

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The Hybrid Integration of a Multistage Active Bandpass Filter/Amplifier

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Abstract—This paper describes the fabrication, characterization, and analysis of a hybrid microcircuit to be used as a signal amplifier and conditioner for an IR tracking system.

The entire circuit is integrated on a 1 X 2-in alumina substrate using thick-film resistors and conductors, some chip resistors in critical locations, chip capacitors, and monolithic integrated-circuit (IC) operational-amplifier (op-amp) chips. Fig. 1 shows a block diagram of the entire circuit. The transfer functions of each of the stages is derived. The predicted gain peak and the shape of the measured bandpass agree well with experimental results. The computer simulation using an op-amp "macromodel" [1] gives results very closely resembling the measured bandpass, and underscores the utility of computer circuit simulations in IC development. Stability and hybrid layout considerations are discussed.

The noise figure is measured as a function of frequency for the given system source impedance of 5 MΩ and also for 0.5 MΩ to indicate the dependence of the noise figure on source resistance. The dominant sources of noise in the amplifier/filter and low-noise design considerations are discussed.

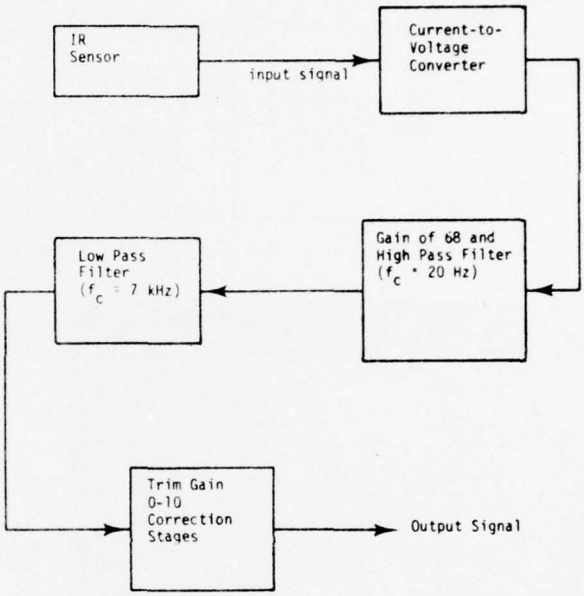

Fig. 1. Hybrid-microcircuit functional diagram.

I. INTRODUCTION

The purpose of this paper is to describe the fabrication, characterization, and analysis of a thick-film hybrid microelectronic circuit to be used as a bandpass filter and amplifier. The original circuit design was done by the U.S. Army Missile Command as part of an IR tracking system and was originally fabricated using discrete components hard-wired together in breadboard fashion.

The amplifier/filter as presented in this paper was integrated on a 1 X 2-in alumina substrate using thick-film resistors and conductors, some chip resistors in critical locations, chip capacitors, and monolithic integrated-circuit (IC) operational-amplifier (op-amp) chips.

Fig. 1 shows a block diagram of the entire circuit. The IR sensor is a silicon p-n diode designed to detect light from a laser source. The photo-current signal from the IR sensor is converted to a voltage signal by the first stage and amplified by the second stage, which also acts as a high-pass filter with a low-frequency −3-dB point of 20 Hz. The third and fourth stages of the amplifier/filter are unity-gain low-pass filters which are designed together as a Chebychev filter with a 0.1 ripple. The upper −3-dB frequency of these two stages is 7 kHz. The final two stages of the circuit are used for gain adjust and dc output voltage offset adjust.

Fig. 2. shows the electrical schematic of the amplifier/filter. Fig. 3 is a photograph of the completed thick-film hybrid circuit showing all components except capacitor C_c, the coupling capacitor between stages one and two, and the two trim potentiometers used for gain adjust and offset voltage adjust in the last two stages. Due to size, these components were mounted on the external printed-circuit board as indicated in Fig. 4. Four amplifier/filters are mounted on one laminated printed-circuit board[1] to complete a four-quadrant IR detector system.

The layout of the hybrid circuit proceeded through several redesigns in order to meet the specifications required. The physical size was constrained to a 1 X 2-in alumina substrate.

Manuscript received June 4, 1976; revised July 15, 1976. This work was carried out at the Hybrid Microelectronic Facility of the U.S. Army Missile Command (AMICOM) in Huntsville, AL, with support from the Department of Electrical Engineering of Auburn University under U.S. Army Contract DAAH01-76C-0328.

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[1]Each circuit-board part was double sided. The completed board has four layers of conductor and plated-through vias.

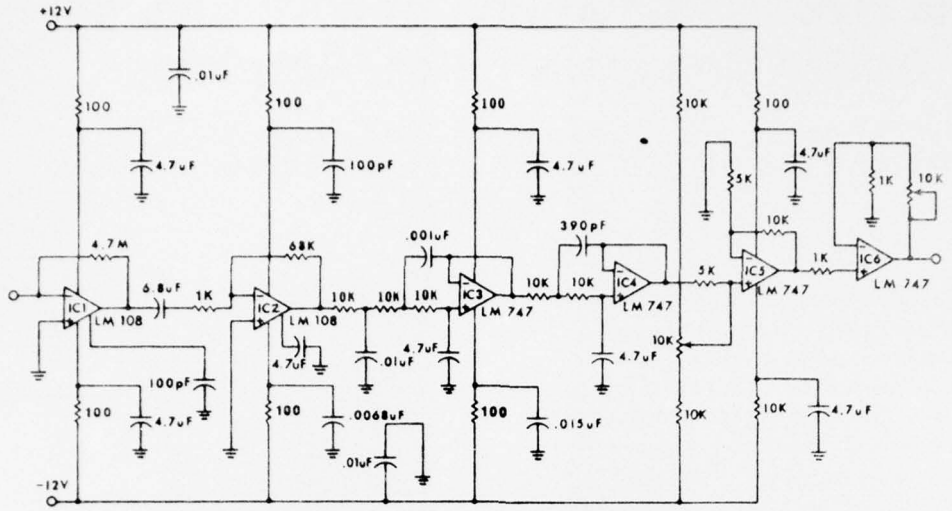

Fig. 2. Electrical schematic of the hybrid filter/amplifier.

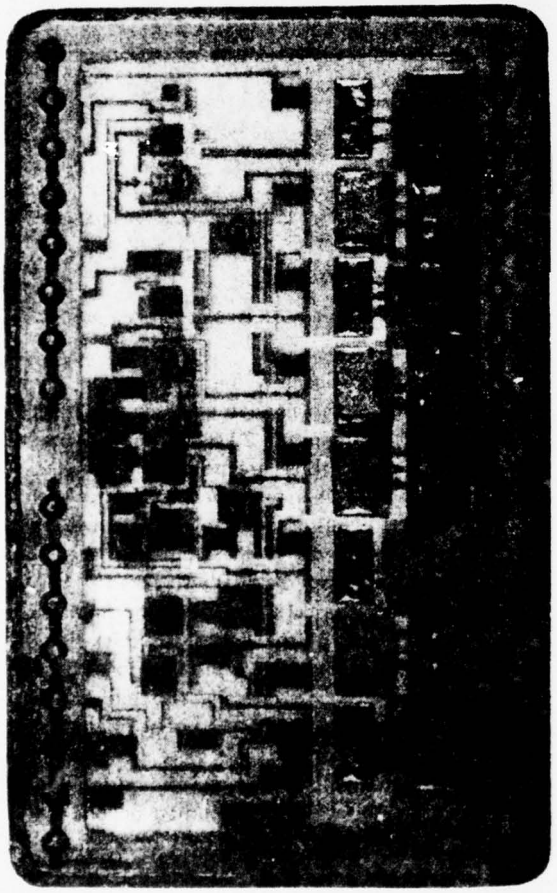

Fig. 3. Photograph of the hybrid filter/amplifier mounted in a metal package with the lid removed.

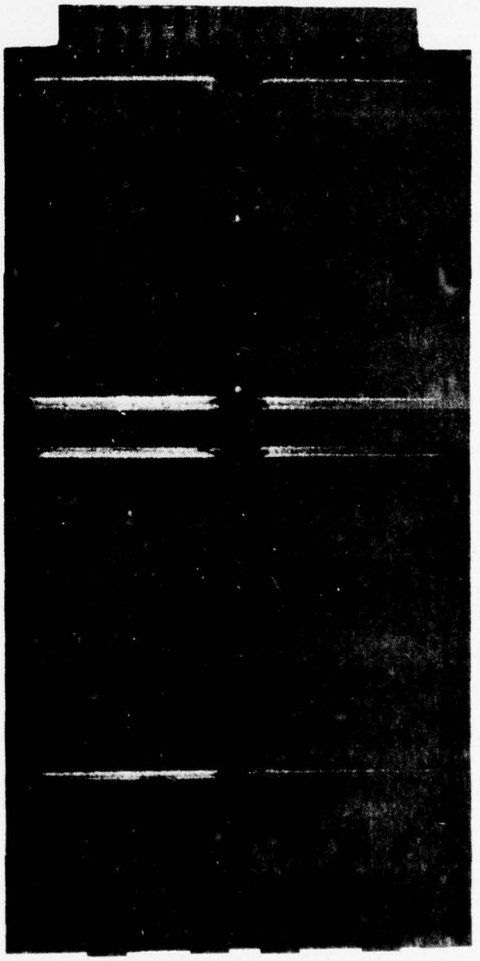

Fig. 4. Photograph of a system of four hybrid amplifier/filter circuits mounted on a multilevel printed-circuit board.

The initial design concept was to split the circuit into two separate packages with *all* the capacitors mounted externally on the printed-circuit board. Cross coupling between the large external capacitors and the two hybrid packages caused circuit instabilities and made the corner frequencies of the filter difficult to reproduce accurately. Hence, a single-package

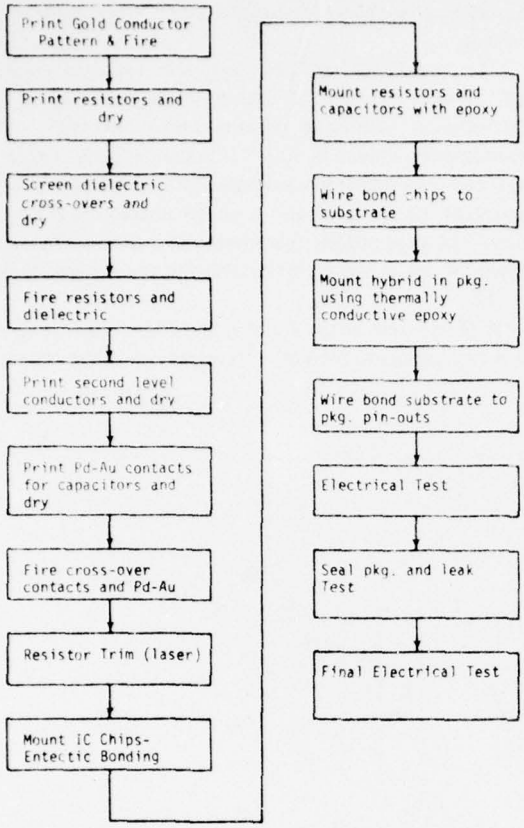

Fig. 5. Thick-film hybrid-circuit fabrication process sequence.

design as described herein evolved as an acceptable solution to the physical-size/electrical-performance constraints. In an attempt to optomize circuit layout, an automatic computer routing and design program was next used to generate a new layout.[2] The resulting hybrid-circuit layout was suitable for a 1 X 1-in alumina substrate, but required three separate conductor layers for its implementation. Because of the need for high reliability with simultaneous ease of fabrication, it was decided not to use a three-level metallization configuration. Thus the computer-aided layout was not used in its original form but was modified by hand to obtain the final layout.

The hybrid amplifier/filter was fabricated using standard thick-film hybrid techniques. The process sequence that was used is shown in Fig. 5.

II. ELECTRICAL ANALYSIS

Introduction

A functional block diagram of the amplifier/filter is shown in Fig. 1. The infrared sensor is a reverse-biased junction detector with an impedance of 4 - 5 MΩ. The first stage of the system is an op-amp circuit operating as a current-to-voltage converter and is capable of detecting current signals down to the picoampere range. The second stage provides a voltage gain of 68 and rejects the low-frequency signal components below its corner frequency of 23 Hz. The next section is a low-pass network designed to cut off sharply at the cutoff frequency, 6.28 kHz. The low-pass section is composed of two op-amp circuits, a three-pole active filter, followed by a two-pole active filter. The final stages are for gain adjustment and dc offset correction.

[2] This work was performed by Algorex Corporation.

TABLE I

LM108 and LM747 Op-Amp Noise Data Used in the Noise Analysis

f(Hz)	E_{n1}(nV)	I_{n1}(pA)	E_{n2}(nV)	I_{n2}(pA)
5	60	.15	100	10
10	41	.10	40	6
30	39	.04	30	4.5
100	34	.015	28	3.5
1K	32	.015	25	2.5
7.5K	31.5	.015	25	2.5
10K	31	.015	25	2.5
15K	31	.015	25	2.5
20K	31	.015	25	2.5
25K	31	.015	25	2.5

Theory

The schematic diagram of the entire filter/amplifier is shown in Fig. 2. The frequency-shaping sections are stages two, three, and four.

Stage two provides a single-pole high-pass filter, with the corner located at 23 Hz. The voltage gain for the second stage, assuming infinite op-amp gain, is

$$A_2(s) = -\frac{R_7}{R_4}\left(\frac{sC_cR_4}{1+sC_cR_4}\right) \tag{1}$$

where the component values are given in Table I.

The third stage provides a three-pole low-pass filter with a voltage gain of

$$A_3(s) = \frac{1}{s^3A_1 + s^2B_1 + sC_1 + 1} \tag{2}$$

where

$$A_1 = R_8C_7R_{10}C_8R_9C_9 \tag{3}$$

$$B_1 = R_8C_7R_9C_9 + R_8C_7R_{10}C_9 + R_{10}C_8R_9C_9 + R_8C_9R_{10}C_8 \tag{4}$$

$$C_1 = R_8C_7 + R_9C_9 + R_{10}C_9 + R_8C_9\,. \tag{5}$$

The magnitude of $A_3(s)$ versus frequency begins to roll off early and is down by a factor of 3 dB at 3 kHz as shown in Fig. 6.

The fourth stage is a two-pole low-pass filter, which is designed along with the third stage by assuming a Chebyshev filter with a 0.1-dB ripple. The magnitude of the transfer function of stage four increases with frequency and closely compensates for the decrease of the third stage to give a total response which is flat up to the cutoff frequency [2]. Above the cutoff frequency the gain decreases rapidly at a rate of 42 dB per octave.

The voltage gain of the fourth stage is

$$A_4(s) = \frac{1}{S^2A_1' + SB_1' + C_1' + 1} \tag{6}$$

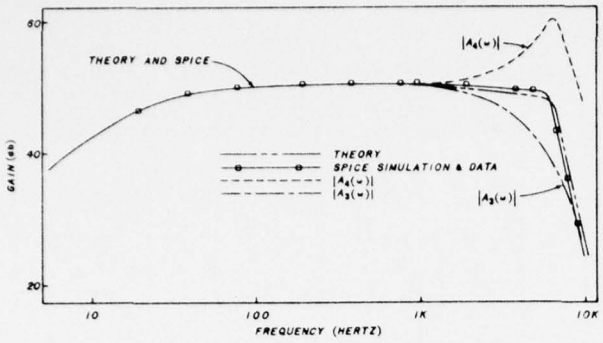

Fig. 6. Frequency response for the amplifier/filter showing experimental data, SPICE computer simulation, and hand calculations.

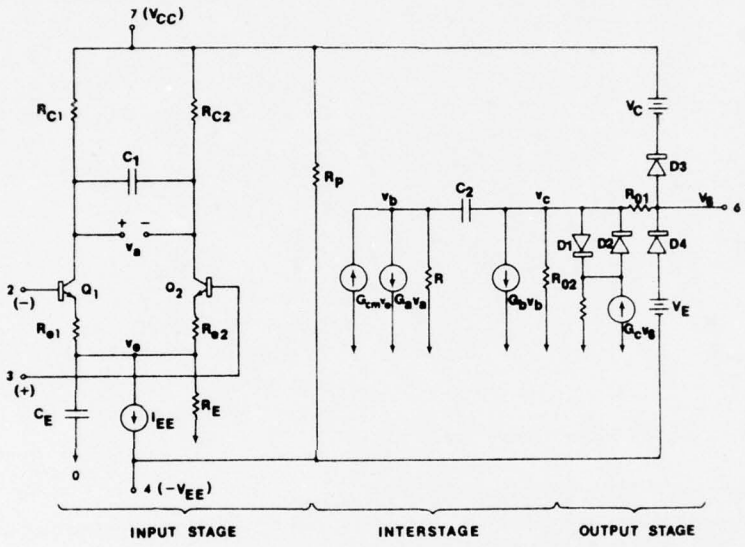

Fig. 7. Circuit diagram of the op-amp macromodel.

where

$$A_1' = R_{13}C_{13}R_{14}C_{12} \quad (7)$$

$$B_1' = R_{13}C_{13} + R_{14}C_{13}\,. \quad (8)$$

The total frequency shaping of the amplifier is determined by the magnitude of the product of $A_2(s)$, $A_3(s)$, and $A_4(s)$. Plotting this product versus frequency gives the theoretical plot shown in Fig. 6 when multiplied by the constant gain factor of stages one, five, and six. The dashed curves indicate the normalized transfer characteristics of stages three and four, and show how these two stages work together to give a total response approximately flat up to the high-frequency corner, followed by a rapid fall.

Computer Simulation

A computer circuit simulation was performed on the hybrid amplifier/filter to check the dc bias conditions and verify the ac bandpass characteristics. The program SPICE [3] (simulation program with integrated-circuit emphasis) was used to perform the analysis. This program offers a number of features which make it useful for hybrid IC analysis. SPICE will perform all three modes of simulation, dc, ac, and transient; it contains a subcircuit capability and has "built-in" device models.

The circuit of Fig. 2 contains two types of op-amps, the LM108 and the LM747. The op-amps are modeled using the macromodel technique presented by Boyle *et al.* [1]. The macromodel shown in Fig. 7 is approximately a factor of six less complex than the original op-amp circuit, yet provides excellent modeling of the terminal characteristics of the op-amp. The macromodel parameters are derived from the data sheets of the above op-amps utilizing the procedure described in [1].

A SPICE simulation for the first four stages was performed and the computer-predicted frequency response for the hybrid IC is also shown in Fig. 6. The simulation includes the effects of parasitic capacitance at critical high-impedance nodes, the effect of coupling through supply lines, and, most importantly, the effect of finite and frequency-dependent op-amp open-loop gains. Notice the SPICE simulation shows significantly more peaking near the high-frequency corner than does the theoretical analysis. The origin of this discrepancy was traced to the fourth stage.

The two-pole active filter of stage four has a theoretical gain peak at 6.5 kHz, assuming infinite op-amp gain. The SPICE simulation models the effect of finite op-amp gain and the gain peak is found to shift slightly lower to 5.9 kHz. The effect of this shift on the total filter response is a slight peaking near the corner and a slightly lower corner frequency.

Experimental Data

The data points in Fig. 6 show experimental measurements on a typical hybrid amplifier/filter unit (number SNB035). Note the excellent agreement between the SPICE simulation and the experimental data points. The computer simulation correctly predicted the small gain peak near the high-

frequency corner and gave an accurate modeling of the gain over the frequency range of 5 Hz - 10 kHz.

III. NOISE ANALYSIS AND PERFORMANCE

Introduction

The hybrid active bandpass filter/amplifier is required to detect minimum signal levels of 10^{-6} V within its −3-dB bandpass. In this section, an analysis of the capability of the circuit in detecting low-level signals is presented along with experimental data to substantiate the analysis. The components which limit the low-signal-level performance of the circuit are identified.

Noise Analysis and Modeling

The noise performance of a multistage amplifier has been treated in detail in numerous articles and texts and only the essentials will be presented here as needed. The reader is referred to [4] and [5] for further reading on the subject.

A useful technique to characterize the noise performance of an amplifier is to express the noise of the amplifier and external resistors in terms of an equivalent input noise-voltage source e_{ni}. The equivalent input noise voltage is the rms voltage that one must apply to the input of a *noiseless* amplifier to get the same output noise as would normally be measured at the output. Thus if e_n is the equivalent input noise of the amplifier (rms) and e_s is the noise of the source resistor (R_S), then

$$e_{ni}^2 = e_n^2 + e_s^2. \tag{9}$$

The noise in amplifiers such as op-amps is usually modeled by two noise sources: a noise current I_n and a noise voltage E_n. The noise voltage is the equivalent input noise voltage with R_s = O and the noise current is the equivalent input noise current with R_s very large. The total equivalent input noise of the amplifier e_n can be expressed as

$$e_n^2 = E_n^2 + I_n^2 R_s^2 . \tag{10}$$

The output noise is composed of two components: the noise from the source resistor and the noise from the amplifier. A measure of the amplifier's contribution to the total output noise is given by the noise figure of the amplifier defined as

F = total output noise power divided by the output noise power due to the source resistance alone, or total mean-square output noise voltage divided by the mean-square output noise voltage due to the source resistor alone;

that is,

$$F = \frac{e_{ni}^2 A_v^2}{e_s^2 A_v^2} = \frac{e_n^2 + e_s^2}{e_s^2} = 1 + \frac{e_n^2}{e_s^2} \tag{11}$$

where A_v is the voltage gain of the amplifier.

The noise of the source resistor will generally be composed of two parts: thermal noise e_s^2 and excess noise e_f^2. Using Nyquists' Theorem [4] for the thermal noise,

$$e_s^2 = 4kTR_s\Delta f \tag{12}$$

where

- k Blotzmann's constant;
- T absolute temperature;
- R_s source resistance;
- Δf noise bandwidth.

Excess noise in resistors has been experimentally determined to follow a relationship similar to

$$e_f^2 = \frac{K_1 I_{dc}^2}{f} . \tag{13}$$

This type of noise is also known as $1/f$ or flicker noise. This type of noise is usually only important in carbon composition and other "grainy" resistors such as thick-film resistors. It is usually negligible in thin-metal-film resistors.

When several amplifier stages are cascaded together, the noise figure of the entire assembly is given by Friiss' Law [5]:

$$F_{TOT} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \tag{14}$$

where the F_i's are the noise figures for each stage and G_i's are the maximum available power gain for each stage:

$$G_i \triangleq \left(\begin{array}{l} \text{amplifier open-} \\ \text{circuit voltage} \\ \text{gain} \end{array} \right)^2 \cdot \frac{R_s}{r_o} \tag{15}$$

where r_o is the output resistance of the amplifier. Thus, even though the noise figure can be $\gg 1$, if each stage of a cascaded amplifier has a large power gain, the noise performance of the system is determined by the first stage and $F_{TOT} \approx F_1$. It becomes very important to have a low-noise first stage.

In order to develop a complete theoretical model to predict the noise of the circuit in Fig. 2, detailed knowledge of the complete noise performance of all the resistors and operational amplifiers would be necessary. Such data is usually available only by experiment. The theoretical prediction of flicker noise is particularly difficult because of the fabrication dependence of constants like K_1 in (13). However, the above theory can be successfully used, along with experimental data and appropriate simplifying assumptions, to evaluate the noise performance of an amplifier and to determine those factors which limit the noise performance. In the next section, experimental noise data are presented, and, in the subsequent section, the above theory is used to analyze the experimental results.

Experimental Results

The noise performance of the circuit in Fig. 2 was determined for $R_s = 5\ \text{M}\Omega$ and $R_s = 0.5\ \text{M}\Omega$ using the test setup shown in Fig. 8. This technique is widely known as the "comparison with a sinusoid" technique and involves using an input sinusoidal signal (set at the center frequency of the spectrum analyzer) as a reference signal to measure the equivalent input noise of the circuit under test. Details of the technique can be found in [6] and [7].

The results from the experimental measurements are plotted in Figs. 9 and 10. Fig. 9 is a plot of equivalent input noise voltage versus frequency. This plot gives a vivid indication of the sensitivity of the circuit to low-level signals. As can be seen, over the passband the circuit can detect signals less

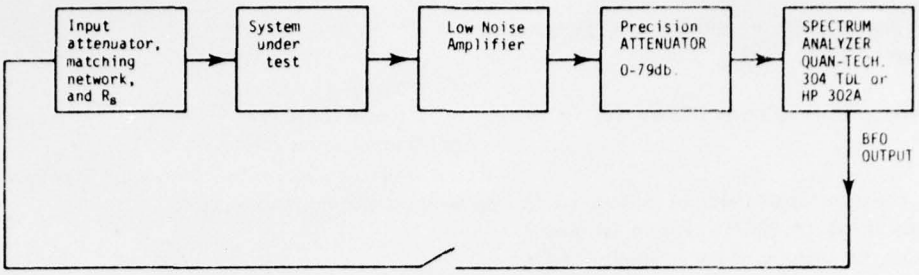

Fig. 8. Test setup for noise measurements.

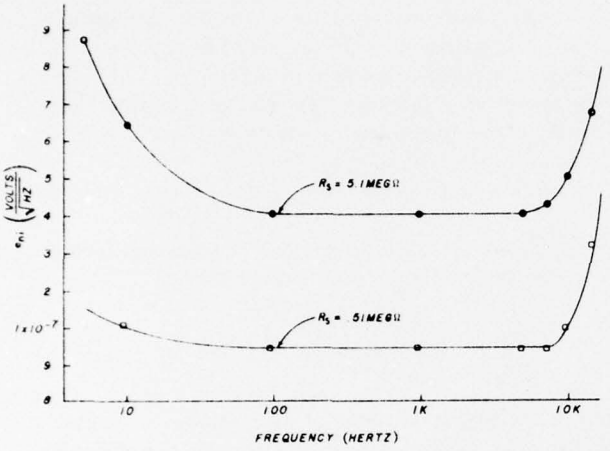

Fig. 9. Equivalent input noise voltage versus frequency.

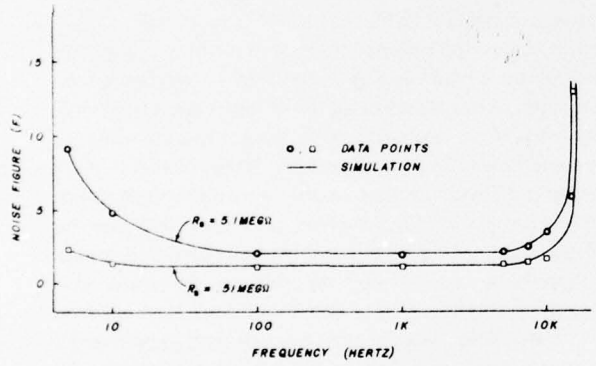

Fig. 10. Noise figure versus frequency.

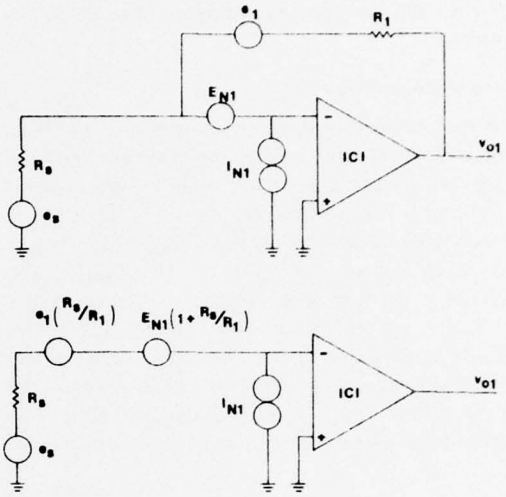

Fig. 11. (a) Noise equivalent circuit of stage one. (b) A rearrangement of this circuit.

than 1 μV with a good signal-to-noise ratio. For a source resistance of 5 MΩ at 1 kHz the signal-to-noise ratio for a 1-μV input would be

$$\frac{S+N}{N} = \frac{10^{-12} + 16 \times 10^{-14}}{16 \times 10^{-14}} = \frac{1.16 \times 10^{-12}}{1.6 \times 10^{-13}} = 7.25 \quad (16)$$

where S is the mean-square input signal voltage and N is the mean-square equivalent input noise voltage e_{ni}^2. Fig. 9 also indicates that the noise performance improves substantially by reducing R_s. A reduction in R_s by a factor of ten reduces the midband equivalent input noise voltage by 4.2.

The frequency dependence of e_{ni} is also evident in Fig. 9. Outside the −3-dB passband, the noise increases dramatically. At low frequencies the increased noise is due to both flicker noise and gain roll-off caused by the coupling capacitor between stages one and two in Fig. 2. At high frequencies the increased noise is due to gain roll-off in stages three and four.

The data of Fig. 9 were converted to the noise figure using (11) and were replotted in Fig. 10. This data along with (14) for F_{TOT} will be used to investigate the performance of the circuit.

Analysis of Performance

According to Friiss' Law, equation (14) the noise performance will be determined by the first stage as long as the G_i's are sufficiently large. In this section, expressions for the available power gain and noise figure for each stage of the amplifier/filter will be determined.

Stage One

The important sources of noise in stage one are the equivalent input noise of the LM108 op-amp and the resistor noise from R_s and R_1. Fig. 11(a) shows this stage with noise generators. Fig. 11(b) shows a noise equivalent circuit which is just a rearrangement of the circuit of Fig. 11(a). The output noise is the same in both cases.

Using Fig. 11, the equivalent input noise for stage one is

$$e_{ni}^2(1) = e_s^2 + e_F^2\left(\frac{R_s^2}{R_1^2}\right) + E_{n1}^2\left(1+\frac{R_s}{R_1}\right)^2 + I_{n1}^2 R_s^2 \quad (17)$$

where $e_s^2 = 4kTR_s\Delta f$, $e_F^2 = 4kTR_1 f$, and E_{n1}^2 and I_{n1}^2 are the equivalent input noise voltage and noise current for the LM108. Typical values of E_{n1}^2 and I_{n1}^2 can be obtained from data sheets provided by National Semiconductor. However, care must be taken in using the data provided in data sheets as the noise performance of op-amps will vary considerably between units and will be a function of supply voltages. Most data sheets give noise data at a ±15-V supply only. For accurate results, E_{n1} and I_{n1} must be measured experimentally under the correct bias conditions.

The excess noise in R_s and R_1 has been neglected in (17) as low-noise thin-metal-film resistors were used in the circuit. Noise from R_1 would be detrimental to the noise performance of the circuit and thus a thin-film chip resistor was used in the hybrid layout rather than a thick-film resistor. Thick-film resistors tend to be very noisy [6]. Using (12), the noise figure for stage one is

$$F_1 = 1 + \frac{R_s}{R_1} + \frac{E_{n1}^2\left(1 + \frac{R_s}{R_1}\right)^2 + I_{n1}^2 R_s^4}{K_1 R_s} \qquad (18)$$

where $K_1 = 4kT = 1.61 \times 10^{-20}$ W, k is Boltzmann's constant, and T is the absolute temperature. The maximum available power gain for stage one is

$$G_1 = \left(\frac{R_1}{R_s}\right)^2 \cdot \frac{R_s}{r_{o1}} = \frac{R_1^2}{R_s r_{o1}} \qquad (19)$$

where r_{o1} is the output resistance of stage one. This parameter is also available from LM108 data sheets. G_1 will depend on R_s. For the case of $R_s = 5.1$ MΩ, $G_1 \approx 10^6$. Due to this large value of G_1, the noise figure inside the passband of the filter will be determined by stage one and for the LM108 will be very close to two, as the noise contribution from the LM108 will be small compared to the noise of resistors R_s and R_1.[3]

Stage Two

The noise equivalent circuit of stage two is shown in Fig. 12. For this circuit, the equivalent input noise voltage is

$$e_{ni}^2(2) = e_{ro1}^2 + e_4^2 + e_7^2\left[\left(\frac{r_{o1}+R_4}{R_7}\right)^2 + \frac{1}{\omega^2 C_c^2 R_7^2}\right] + I_{n1}^2\left[(r_{o1}+R_4)^2 + \frac{1}{\omega^2 C_c^2}\right] + E_{n1}^2\left[\left(1+\frac{r_{o1}+R_4}{R_7}\right)^2 + \frac{1}{\omega^2 C_c^2 R_7^2}\right] \qquad (20)$$

where

$e_4^2 = 4kTr_4\Delta f$
$e_7^2 = 4kTr_7\Delta f$
$er_{o1}^2 = 4kTr_{o1}\Delta f.$

[3]This fact is not obvious nor necessarily always true. Experimental data indicated that for the LM108's used in this particular experiment, it was true. It is important to select a low-noise op-amp for the first stage, and, if this is done, the noise performance of stage one will be determined by the noise in R_s and R_1. These should be very-low-noise resistors. In this design a low-noise metal-film resistor was used for R_1. If thick-film processing had been used for R_1, excess noise in R_1 would have made the first-stage low-frequency noise significantly greater as discussed in the paper.

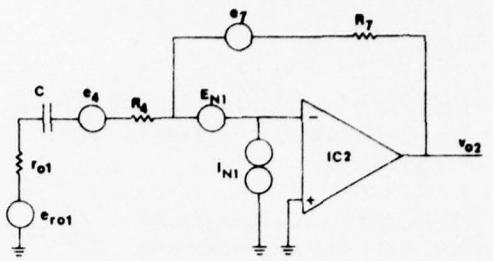

Fig. 12. Noise equivalent circuit of stage two.

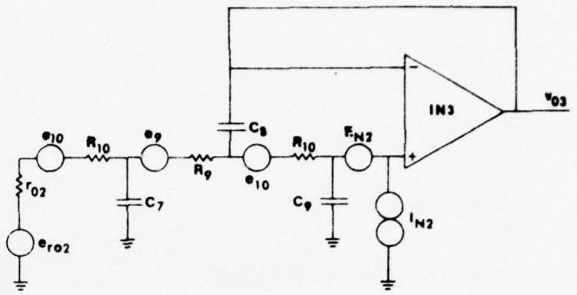

Fig. 13. Noise equivalent circuit of stage three.

From (20), the noise figure for stage two is

$$F_2 - 1 = \frac{R_4}{r_{o1}} + \frac{R_7}{r_{o1}}\left[\left(\frac{r_{o1}+R_4}{R_7}\right)^2 + \frac{1}{\omega^2 C_c^2 R_7^2}\right] + \frac{I_{n1}^2}{K_1 r_{o1}}\left[(r_{o1}+R_4)^2 + \frac{1}{\omega^2 C_c^2}\right] + \frac{E_{n1}^2}{K_1 r_{o1}}\left[\left(1+\frac{r_{o1}+R_4}{R_7}\right)^2 + \frac{1}{\omega^2 C_c^2 R_7^2}\right] \qquad (21)$$

where $r_{o1} \cong 0.1\ \Omega$ when $R_s = 5.1$ MΩ and $r_{o1} \cong 1\ \Omega$ when $R_s = 0.51$ M and

$R_4 = 1$ K
$R_7 = 68$ K
$C_c = 6.8\ \mu$F.

The maximum available power gain for stage two is

$$G_2 = (A_2)^2\left(\frac{r_{o1}}{r_{o2}}\right)\frac{R_7^2 r_{o1}}{R_4^2 r_{o2}\left(1+\frac{1}{\omega^2 C_c^2 R_4^2}\right)} \qquad (22)$$

At low frequencies this term will cause the noise figure F to increase.

Stage Three

The noise equivalent circuit of stage three is shown in Fig. 13. For this circuit,

$$e_{ni}^2 = (e_{ro2})^2 + e_8^2 + e_9^2(1+\omega^2 A'') + e_{10}^2(1+\omega^2 B'' + \omega^4 C'') + e_{n2}^2(1+\omega^2 E + \omega^4 F + \omega^6 G) + I_{n2}^2(H + \omega^2 I + \omega^4 J) \qquad (23)$$

where

$A'' = R_8^2 C_7^2$
$B'' = (R_A C_8 + R_9 C_8 + R_A C_7)^2 = 2R_A R_9 C_7 C_8$
$C'' = R_A C_7 C_8 R_9$
$E = -2\alpha + \beta^2$

$$
\begin{aligned}
F &= \alpha^2 - 2\beta\gamma \\
G &= \gamma^2 \\
\alpha &= R_A C_7 C_9 R_{10} + C_8 C_9 R_{10}(R_A + R_9) + C_9 R_A R_9 C_7 \\
\beta &= C_9 R_{10} + R_A C_7 + C_8(R_A + R_9) + C_9(R_A + R_9) \\
\gamma &= C_8 R_A R_9 C_7 C_9 R_{10} \\
H &= (R_{10} + R_9 + R_A)^2 \\
I &= -2(R_{10} + R_9 + R_A)(C_8 R_9 R_{10} R_A C_7) \\
&\quad + (C_7 R_A R_{10} + C_8 R_9 R_{10} + C_8 R_{10} R_A \\
&\quad + R_9 R_A C_7)^2 \\
J &= (C_8 R_9 R_{10} R_A C_7)^2 \\
r_{o2} &\cong 5\ \Omega \\
R_A &= r_{o2} + R_8 \cong R_8
\end{aligned}
$$

and

$$
\begin{aligned}
F_3 - 1 = {} & \frac{R_8}{r_{o2}} + \frac{R_g}{r_{o2}}(1 + \omega^2 {R_8}^2 {C_7}^2) \\
& + \frac{R_{10}}{r_{o2}}(1 + B''\omega^2 + C''\omega^4) \\
& + \frac{{E_{n2}}^2}{K_1 r_{o2}}(1 + \omega^2 E + \omega^4 F + \omega^6 G) \\
& + \frac{{I_{n2}}^2}{K_1 r_{o2}}(H + \omega^2 I + \omega^4 J) \qquad (24)
\end{aligned}
$$

$$
G_3 = \frac{1}{(1 - \omega^2 M)^2 + (\omega N - \omega^3 P)^2} \qquad (25)
$$

where

$$
\begin{aligned}
M &= R_8 C_7 R_9 C_9 + R_8 C_7 R_{10} C_9 + R_{10} C_8 C_9 R_9 \\
&\quad + R_8 C_9 R_{10} C_8 \\
N &= R_8 C_7 + R_9 C_9 + R_{10} C_9 + R_8 C_9 \\
P &= R_8 C_7 R_{10} C_8 R_9 C_9 .
\end{aligned}
$$

Stage Four

Stage four is similar to stage three. The noise equivalent circuit is shown in Fig. 14. For this circuit,

$$
\begin{aligned}
{e_{ni}}^2(4) = {} & {e_{r_{o3}}}^2 + {e_{13}}^2 + {e_{14}}^2(1 + {B_1}''\omega^2) \\
& + {E_{n2}}^2(1 + \omega^2 E' + \omega^4 F') + {I_{n2}}^2(H' + \omega^2 I') \qquad (26)
\end{aligned}
$$

where

$$
\begin{aligned}
{B_1}'' &= (r_{o3} C_{12} + R_9 C_{12})^2 \\
E'' &= -2\alpha' + (\beta')^2 \\
F' &= (\alpha')^2 \\
\alpha' &= C_{12} C_{13} R_{10}(r_{o3} + R_9) \\
\beta' &= C_{13} R_{10} + (r_{o3} + R_9) C_{12} + C_{13}(R_{o3} + R_9) \\
H' &= (R_{10} + R_9 + r_{o3})^2 \\
I' &= (C_{12} R_9 R_{10} + C_{12} R_{10} r_{o3})^2
\end{aligned}
$$

and the noise figure is

$$
\begin{aligned}
F_4 - 1 = {} & \frac{R_9}{r_{o3}} + \frac{R_{10}}{r_{o3}}(1 + {B_1}''\omega^2) + \frac{{E_{n2}}^2}{K_1 r_{o3}}[1 + \omega^2 E' + \omega^4 F'] \\
& + \frac{{I_{n2}}^2}{K_1 r_{o3}}[H' + \omega^2 I'] . \qquad (27)
\end{aligned}
$$

The above equations were plotted using an HP-2000A digital computer. The resulting theoretical curve is plotted along with the experimental data in Fig. 10. As can be seen, a fairly good fit is obtained between the theory and experiment. A listing of E_n and I_n values used in the simulation is given in Table I. By examining the results of the computer simulation, one can compare the importance of each term contributing to the total noise figure F. In Fig. 15 each component of the noise figure has been plotted using the computer results. The first term in (14), F_1, determines the low-frequency and midband noise performance. Above 5 Hz the low-frequency noise of the LM108 increases faster than the capacitor C_c causes the other noise terms to increase. The fourth term $(F_{4\text{-}1}/G_1 G_2 G_3)$ determines the high-frequency noise performance. The fourth term is always dominant over the third term by at least an order of magnitude. The ultimate sensitivity of the circuit at midband is determined by the noise of stage one and this is set by the thermal noise of R_s and R_1 as indicated in Fig. 15.

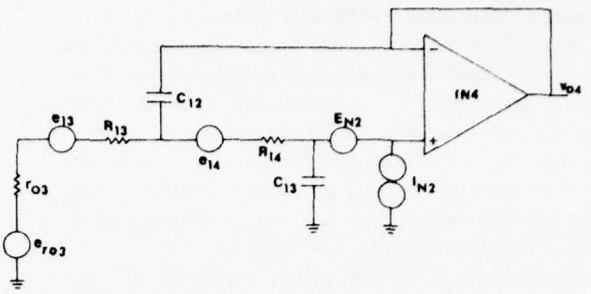

Fig. 14. Noise equivalent circuit of stage four.

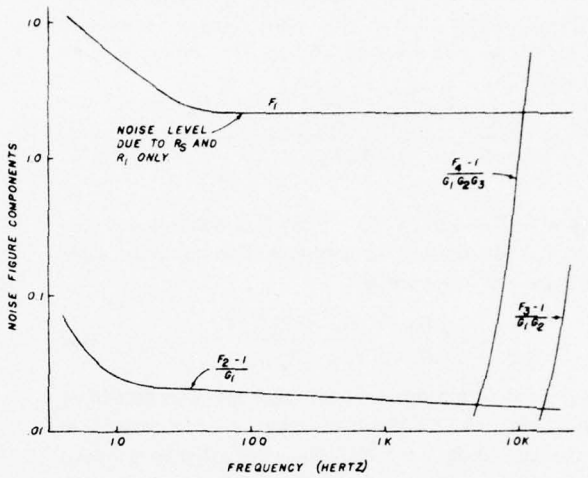

Fig. 15. Noise figure components versus frequency.

IV. SUMMARY

In this paper, an electrical and noise analysis of a thick-film hybrid amplifier/filter has been given. Simulation of the performance of the amplifier has been accomplished using an existing computer program —SPICE. This result was compared to both experimental data and simple theoretical calculations. The accuracy and adequacy of computer simulation has been demonstrated. The noise performance of the circuit was analyzed using noise-figure concepts and was found

to be in agreement with experimental results. It is hoped that the techniques demonstrated in this work may prove useful to others involved in the design and analysis of hybrid amplifiers.

ACKNOWLEDGMENT

The authors would like to acknowledge the work of C. Jennings who did the original circuit design, P. Wanco who did much of the hybrid layout, and the engineers and technicians of the Hybrid Microelectronic Laboratory, MICOM, Huntsville, AL.

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Part 2

COMPUTER-AIDED THERMAL ANALYSIS OF A HYBRID MULTISTAGE ACTIVE BANDPASS FILTER/AMPLIFIER

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T. D. Slagh, and V. W. Ruwe

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Computer-Aided Thermal Analysis of a Hybrid Multistage Active Bandpass Filter/Amplifier

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Abstract—This paper describes the thermal analysis of a hybrid microcircuit to be used as a signal amplifier and conditioner for an IR tracking system. The details of circuit fabrication and an analysis of the electrical and noise performance of the circuit have been presented in a previous paper [1]. It is the purpose of this paper to describe the use of computer-aided analysis to determine the thermal performance of the circuit and to present a computer-aided approach to the thermal design of hybrid microelectronic circuits.

Thermal analysis and measurements are made, revealing the temperature distribution and power-dissipating capability. These results also provide design guidelines for the layout of heat-dissipating devices such as amplifier chips. Package convection and radiation as well as internal heat conduction are modeled using node point analysis. Temperature measurements provide verification of the thermal models.

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I. INTRODUCTION

The development of a complex hybrid microelectronic circuit requires many diverse skills. The development team must perform electronic circuit design, simulation, and breadboard testing as well as topological layout and hybrid device construction and testing. Important phases in the development cycle, which are sometimes neglected, are electronic noise analysis and thermal simulation.

A proposed interactive computer-aided-design system to assist the development team in the electronic-simulation, topological-layout, and thermal-simulation phases has been described [2]. The thermal-analysis models and algorithms of this paper are well suited to computer implementation.

The purpose of this paper is to describe the thermal analysis of a thick-film hybrid microelectronic circuit to be used as a bandpass filter and amplifier. The original circuit design, which was done by the U.S. Army Missile Command as part of an IR

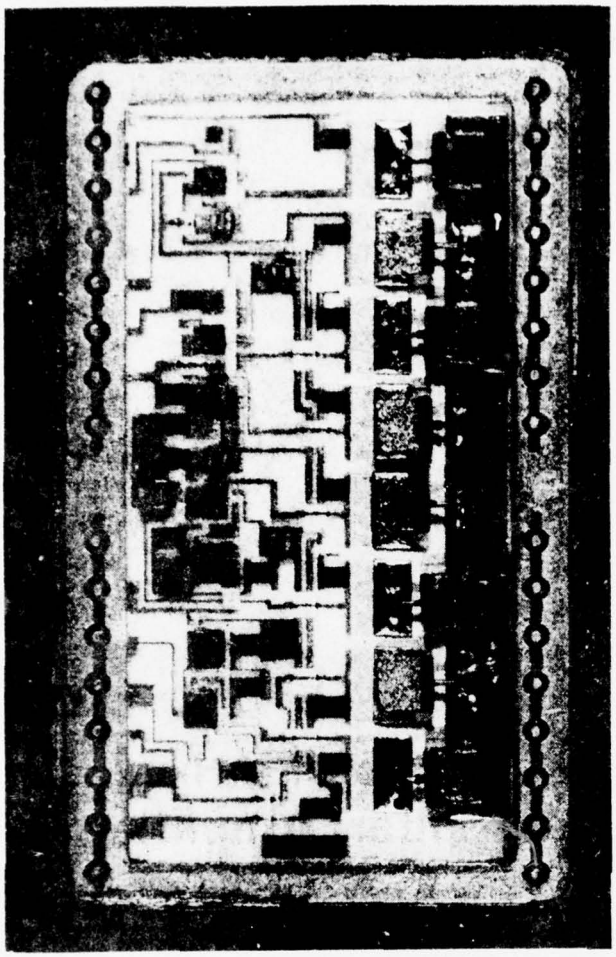

Fig. 1. Photograph of the hybrid filter/amplifier in a 32-pin dual-in-line package.

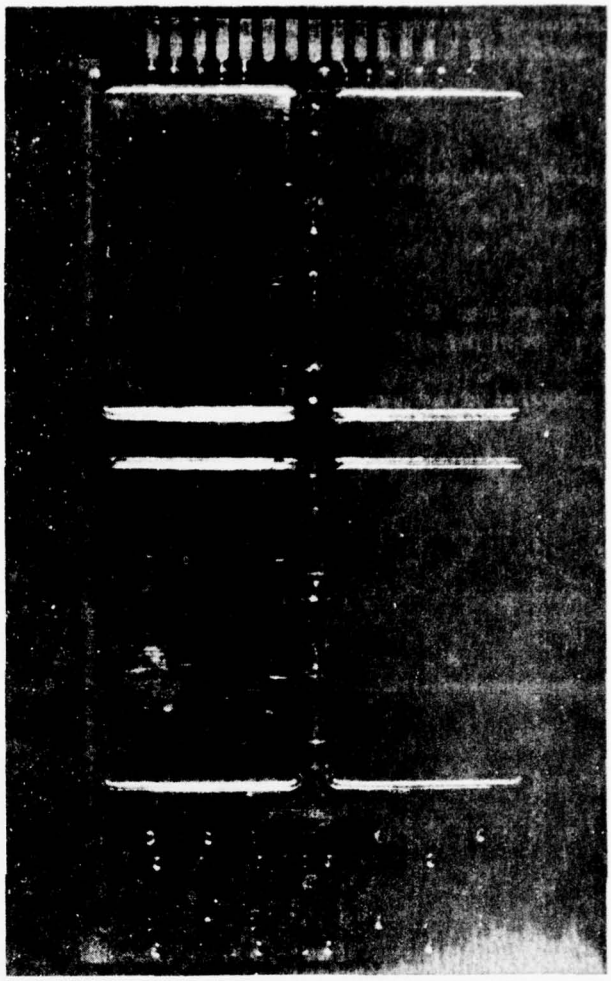

Fig. 2. Photograph of a system of four hybrid filter/amplifiers mounted on a multilevel printed-circuit board.

tracking system, was originally fabricated using discrete components hard-wired together in breadboard fashion. The amplifier/filter was integrated on a 1 X 2-in alumina substrate using thick-film resistors and conductors, some chip resistors in critical locations, chip capacitors, and monolithic IC operational amplifier chips, as shown in Fig. 1. The completed circuit was sealed in a 32-pin dual-in-line package and mounted on a multilevel printed-circuit-board assembly as shown in Fig. 2 [1]. In this paper, a simplified thermal model for hybrid microelectronic circuits is developed and then experimentally verified. The purpose is not to obtain an exact model, but rather to find a model which approximates the "hot spots" on the circuit so that the layout designer can identify possible thermal problem areas.

II. THERMAL MODEL FOR HYBRID CIRCUITS

This is a description of a simplified thermal model for hybrid microelectronic circuits to be used with the Chrysler improved numerical differencing analyzer (CINDA) thermal-analysis program [3]. A sketch of the hybrid circuit is shown in Fig. 3. The model shown in the figure assumes that the package is mounted securely to an infinite heat sink (node 3). Also a convection node (node 2) and a radiation node (node 1) are included; node 8 is at the top of the circuit. Each heat generating element in the hybrid circuit is modeled as four nodes; one in the source itself, and one directly under the source in each of the following: the substrate, the substrate bonding epoxy, and the header. Hence the total number of nodes for a hybrid circuit is

$$N_T = 4N_s + 8 \tag{1}$$

where N_s is the total number of heat sources. N_T is limited to 4000 by the CINDA program.

Thermal Conductances

The CINDA program requires as input data the thermal conductance C_{ij} between physically adjacent nodes in the model.

Thermal conductance and resistance may be calculated by

$$C_{ij} = \frac{A_{ij}}{d} \times k \tag{2}$$

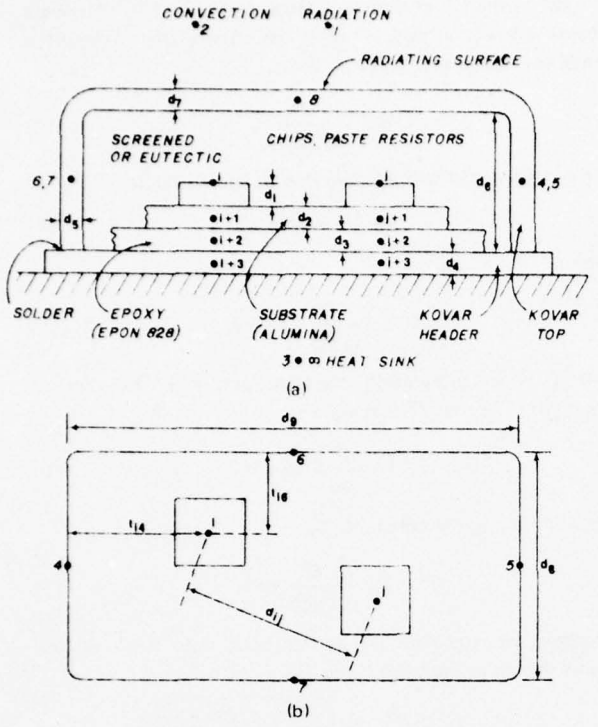

Fig. 3. Physical layout of the hybrid circuit used in the thermal analysis. (a) Side view. (b) Top view.

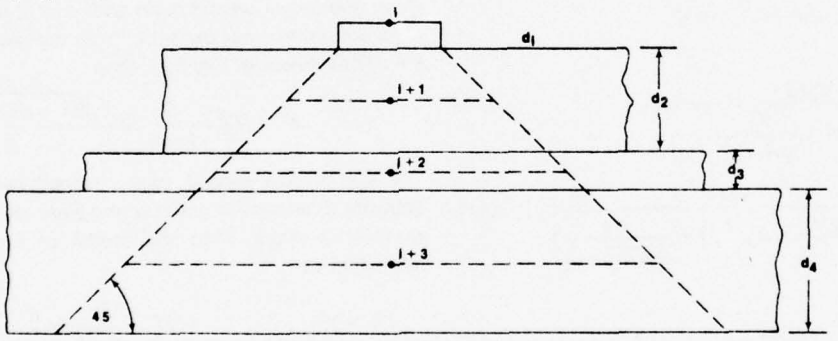

Fig. 4. Model for thermal analysis.

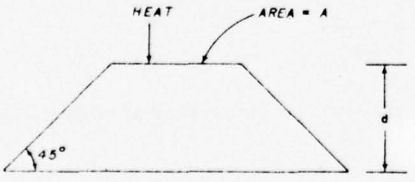

Fig. 5. Spreading model of Balents.

and

$$\theta_{ij} = \frac{d}{kA_{ij}} = \frac{1}{C_{ij}} \tag{3}$$

where A_{ij} is the effective cross-sectional area of conducting medium, d is the path length, and k is the thermal conductivity of the medium. If there is a discontinuity in materials between the nodes, then

$$C_{ij} = \frac{1}{\frac{1}{C_i} + \frac{1}{C_j}} \tag{4}$$

and

$$\theta_{ij} = \theta_i + \theta_j \tag{5}$$

where C_i is the conductance in one material; C_j, in the other. Consider node i, $i+1$, etc., in Fig. 4. One may compute the thermal resistances for these nodes by using the spreading model of Balents [4]. This model assumes a 45° heat spreading area as shown in Fig. 5. Fig. 5 shows a single layer of material with heat entering a square area on the top surface. Employing the spreading model, the thermal conductance through the layer is

$$C = \frac{kA}{d}\left(1 + \frac{2d}{\sqrt{A}}\right). \tag{6}$$

Let us examine the thermal resistance from node i to $i+1$ as shown in Fig. 6(a). The heat is first carried through the chip to the substrate by a resistance

$$\theta_1 = \frac{d_i}{k_i A_i}. \tag{7}$$

If we assume that node $i+1$ is in the middle of the alumina substrate, then a second resistance term must be added using the spreading model:

$$\theta_2 = \frac{d_2/2}{k_s A_i\left(1 + \frac{d_2}{\sqrt{A_i}}\right)}. \tag{8}$$

Hence the resulting expression is

$$\theta_{i,i+1} = \frac{d_i}{A_i k_i} + \frac{d_2/2}{k_s A_i\left(1 + \frac{d_2}{\sqrt{A_i}}\right)}. \tag{9}$$

One may use the same model to generate the remaining thermal resistances using Fig. 6(b) and (c). Hence

$$\theta_{i+1,i+2} = \frac{d_2/2}{k_s A_{i+1}\left(1 + \frac{d_2}{\sqrt{A_{i+1}}}\right)} + \frac{d_3/2}{k_E\left(\sqrt{A_{i+1}} + d_2\right)^2\left(1 + \frac{d_3}{\sqrt{A_{i+1}} + d_2}\right)}$$

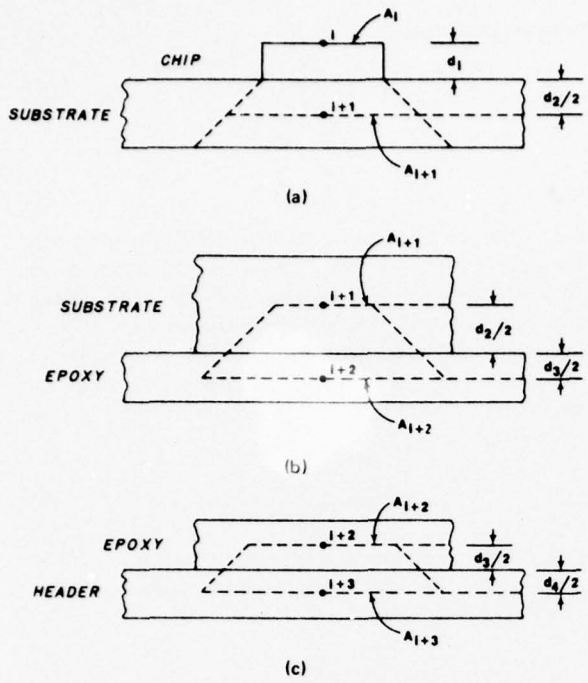

Fig. 6. Multilayer spreading model.

where

$$A_{i+1} = (\sqrt{A_i} + d_2)^2$$

and

$$\theta_{i+2,i+3} = \frac{d_3/2}{k_E A_{i+2}\left(1 + \frac{d_3}{\sqrt{A_{i+2}}}\right)} + \frac{d_4/2}{k_H(\sqrt{A_{i+2}} + d_3)^2\left(1 + \frac{d_4}{\sqrt{A_{i+2}} + d_3}\right)} \tag{11}$$

where

$$A_{i+2} = (\sqrt{A_i} + 2d_2 + d_3)^2$$

and

$$\theta_{i+3,3} = \frac{d_4/2}{k_H A_{i+3}\left(1 + \frac{d_4}{\sqrt{A_{i+3}}}\right)} \tag{12}$$

where

$$A_{i+3} = (\sqrt{A_i} + 2d_2 + 2d_3 + d_4)^2 .$$

The thermal resistance between adjacent nodes in the horizontal layers is formulated in Fig. 7. Since the thermal conductivities of the alumina substrate (0.0236 Btu/min in °F), the epoxy (0.00116 Btu/min in °F), and the Kovar header (0.0154 Btu/min in °F) are relatively different, the epoxy will tend to insulate the substrate and the header. Hence an approximation to the heat transfer between two nodes, say $i+1$ and $j+1$, can be handled as a separate infinite sheet as shown in Fig. 8(a). We assume that source node α resides in a small area, $A_\alpha = \pi a^2$, which is at constant temperature and is emitting a constant power output of Q watts. Then the differential thermal resistance at radius r is

$$d\theta = \frac{dr}{k(2\pi r)h} \tag{13}$$

and the differential temperature due to the source is

$$dT^s = -Qd\theta . \tag{14}$$

Hence

$$T^s = 2\frac{-Q}{2\pi kh} \ln r + K \tag{15}$$

where K is an integration constant and k is the thermal conductivity. At $r=a$, T^s just equals

$$T^s_\alpha = \frac{-Q}{2\pi kh} \ln a + K . \tag{16}$$

Then, eliminating the constant K,

$$T^s = T^s_\alpha - \frac{Q}{2\pi kh} \ln \frac{r}{a} . \tag{17}$$

Suppose we translate the source node α to $-d/2$ on the x axis as shown in Fig. 8(b). Now

$$T^s = T^s_\alpha - \frac{Q}{2\pi kh} \ln \left(\frac{\sqrt{(x + d/2)^2 + y^2}}{a} \right) . \tag{18}$$

If we consider a second drain node β of area $A_\beta = \pi b^2$, extracting a constant power output Q from the sheet, to be located at $x = d/2$ as shown in Fig. 8(c), then

$$T^d = T^d_\beta + \frac{Q}{2\pi kh} \ln \left(\frac{\sqrt{(x - d/2)^2 + y^2}}{b} \right) . \tag{19}$$

The sign of the second term changed because Q is in the opposite direction. If nodes α and β are assumed to coexist on an infinite plane, then the model of Fig. 9 results in the following. Let

$$T^s_\alpha = T^s \Big|_{\substack{x = d/2 \\ y = 0}} = T^s_\alpha - \frac{Q}{2\pi kh} \ln \frac{d}{a} \tag{20}$$

$$T^d_\alpha = T^d \Big|_{\substack{x = -d/2 \\ y = 0}} = T^d_\alpha + \frac{Q}{2\pi kh} \ln \frac{d}{b} . \tag{21}$$

Then, by superposition, the temperature at node α is approximately

$$T_\alpha \doteq T^s_\alpha + T^d_\alpha \tag{22}$$

$$\doteq T^s_\alpha + T^d_\beta + \frac{Q}{2\pi kh} \ln \frac{d}{b} \tag{23}$$

and at node β is approximately

$$T_\beta \doteq T^s_\beta + T^d_\beta \tag{24}$$

$$\doteq T^s_\alpha - \frac{Q}{2\pi kh} \ln \frac{d}{a} + T^d_\beta . \tag{25}$$

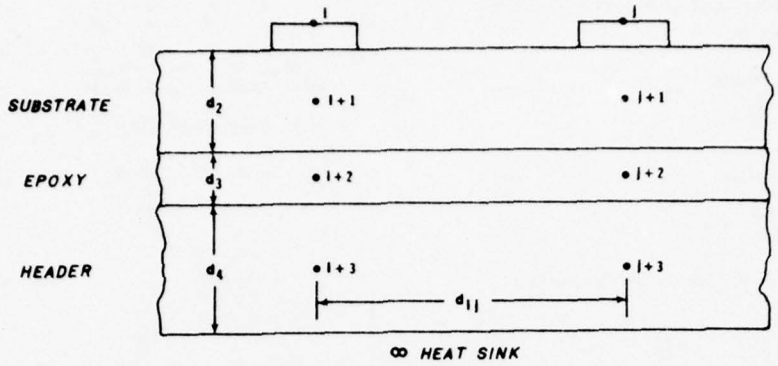

Fig. 7. Lateral node model.

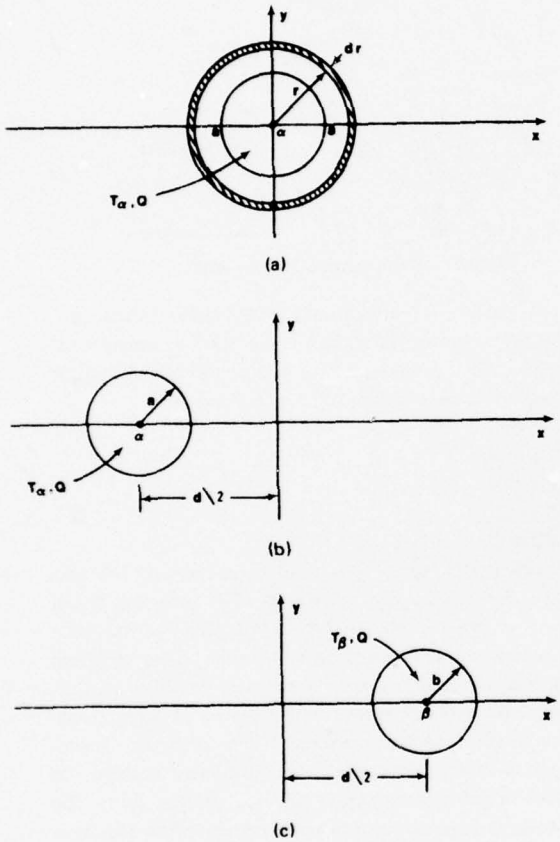

Fig. 8. Sheet-spreading-model derivation.

Consequently, the temperature difference is

$$\Delta T = T_\alpha - T_\beta = \frac{Q}{2\pi kh}\left[\ln\frac{d}{a} + \ln\frac{d}{b}\right] \tag{26}$$

$$= \frac{Q}{2\pi kh}\ln\frac{d^2}{ab} \quad . \tag{27}$$

Hence the thermal conductance C is

$$C = \frac{Q}{\Delta T} = \frac{2\pi kh}{\ln\left(\frac{d^2}{ab}\right)} \quad . \tag{28}$$

This relationship will now be used for the node pairs $(i+1, j+1)$, $(i+2, j+2)$, and $(i+3, j+3)$ or, in general, $(i+k, j+k)$. See Fig. 3.

First we assume that the node areas of constant temperature are approximately A_{i+k} and A_{j+k}, as calculated previously. Then,

$$C_{i+k,\,j+k} = \frac{2\pi k_k\, d_{k+1}}{\ln\left[\dfrac{(d_{ij})^2}{\sqrt{\dfrac{A_{i+k}}{\pi}}\cdot\sqrt{\dfrac{A_{j+k}}{\pi}}}\right]}, \qquad k = 1,3 \tag{29}$$

where $k_1 = k_S$ (alumina), $k_2 = k_E$ (epoxy), $k_3 = k_H$ (Kovar).

Since the Kovar header and top will remain at a relatively constant temperature due to the heat sink, we assume that each node $i+3$, $j+3$, etc., is sufficiently isolated from the sides and top that these thermal conductances can be ignored. That is, the top can be considered to be part of the infinite heat sink, so that nodes 3, 4, 5, 6, 7, and 8 will be at approximately

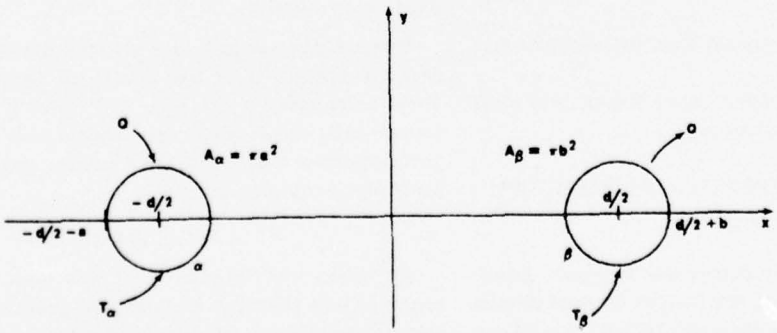

Fig. 9. Sheet spreading model.

the same steady-state temperature. Hence the conductances from node 3 to the side nodes will be

$$C_{3,4} = C_{3,5} = \frac{d_5 d_8}{\frac{d_6}{2} + d_4} k_H \tag{30}$$

$$C_{3,6} = C_{3,7} = \frac{d_5 d_9}{\frac{d_6}{2} + d_4} k_H . \tag{31}$$

From the sides to the package top, the conductances will be

$$C_{4,8} = C_{5,8} = \frac{1}{\frac{1}{\frac{d_5 d_8 k_H}{d_6/2}} + \frac{1}{\frac{d_7 d_8 k_H}{d_9/2}}} \tag{32}$$

$$C_{6,8} = C_{7,8} = \frac{1}{\frac{1}{\frac{d_5 d_9 k_H}{d_6/2}} + \frac{1}{\frac{d_7 d_9 k_H}{d_9/2}}} . \tag{33}$$

Convection

Convection from the vertical and horizontal walls is handled in the CINDA by a temperature-sensitive array of data for h_c, the surface convection coefficient. For natural convection, this coefficient varies as the one-fourth power of the temperature difference between the surface and convection node 2. Since this coefficient is not constant, an initial "guess" of the surface temperature must be included in the data array. This is iteratively corrected by the program.

Radiation

The radiation flow is computed by the CINDA using the Stefan-Boltzmann law. Input data include emissivity, view factor, and radiating area.

Special Case–No Top Cover: If the Kovar top is removed, then nodes 4, 5, 6, 7, and 8 are removed from the model. Hence

$$N_T = 4N_s + 3. \tag{34}$$

Each source i is now able to transfer heat by radiation and convection to nodes 1 and 2.

Convection from a horizontal surface follows the rule

$$C_{i,2} = h_c A_{i+1}$$

$$h_c = 0.27(\Delta t / A_{i+1})^{0.25} \tag{35}$$

where A_{i+1} includes some convection from the substrate surface.

Since A_{i+1} is different for each source i, a data array must be calculated for each individual source.

III. SIMULATION AND EXPERIMENTAL RESULTS

Simulation Results

After the high-gain-amplifier circuit was designed, breadboarded, and physically laid out, the CINDA thermal simulations were used to verify that thermal problems would not occur. From the circuit breadboard and SPICE simulations, the major power sources were identifed as the five operational amplifier chips. The predicted power dissipation in each operational amplifier was determined to be as follows:

IC1 10 mW,
IC2 25 mW,
IC3 100 mW,
IC4 500 mW,
IC5 500 mW.

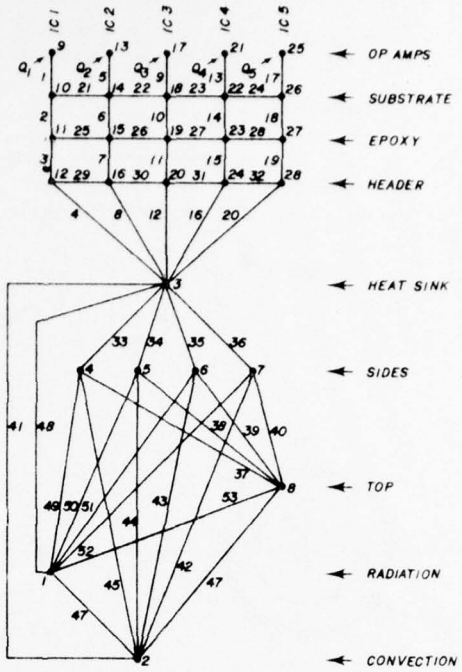

Fig. 10. Node diagram (top on can).

The hybrid-circuit layout was used to determine the area and distance parameters for the model. The resulting node-configuration diagram is shown in Fig. 10. The thermal conductances between nodes are shown in Table I. The resulting CINDA thermal-simulation results are shown in Table II, Column a. Since this configuration is for a sealed package, experimental verification of these results is very difficult. Therefore, a circuit without a covering lid was simulated as shown in Fig. 11. The nodal conductances do not change (only the radiation areas change) from the previous case. The resulting simulation results are shown in Table II, Column b.

Experimental Results

Thermocouple probes were used to experimentally measure device temperatures in the vicinity of certain model nodes. These measurements are shown in Table II, Column c. The experimental values agree reasonably closely with the simulation, indicating that the model is realistic and quite acceptable for design verification purposes.

IV. SUMMARY

We found that, in circuits of this type, placing the five operational amplifiers in a straight line along the largest dimension of the substrate tends to alleviate peak-temperature prob-

TABLE I

Thermal Conductances (Btu/min/°F)

Node	Pair	Conductance	Node	Pair	Conductance
2	3	15.18(Δt).25	15	19	7.92×10^{-6}
2	4	.1027(Δt).25	16	20	.002058
2	5	.1027(Δt).25	17	18	.006925
2	6	.1687(Δt).25	18	19	.006458
2	7	.1687(Δt).25	18	22	.000947
2	8	.7512(Δt).25	19	20	.005494
3	4	.00231	19	23	8.6×10^{-6}
3	5	.00231	20	24	.00225
3	6	.003795	21	22	.006925
3	7	.003795	22	23	.006458
3	12	.02153	22	26	.00174
3	16	.02153	23	24	.005494
3	20	.02456	23	27	1.81×10^{-5}
3	24	.02456	24	28	.00732
3	28	.02456	25	26	.006925
4	8	2.629×10^{-4}	26	27	.006458
5	8	2.812×10^{-4}	27	28	.005494
6	8	6.812×10^{-4}			
7	8	6.812×10^{-4}			
9	10	.00471			
10	11	.005054			
10	14	.000845			
11	12	.004455			
11	15	7.68×10^{-6}			
12	16	0.0020			
13	14	.00471			
14	15	.005054			
14	18	.00087			
15	16	.004455			

TABLE II

Nodal Temperatures (°F)

Node	(a)Simulated Top on Can	(b)Simulated Top off Can	(c)Experimental Top off Can
1	70.0	70.0	70.0
2	70.0	70.0	-
3	70.0	70.1	70.0
4	70.0	-	-
5	70.0	-	-
6	70.0	-	-
7	70.0	-	-
8	70.0	-	-
9	71.4	70.6	70.3
10	71.1	70.5	-
11	70.7	70.4	-
12	70.2	70.1	-
13	72.4	71.3	70.3
14	71.9	70.9	-
15	71.1	70.6	-
16	70.2	70.2	-
17	75.1	72.4	72
18	74.1	71.9	-
19	72.5	71.2	-
20	70.5	70.3	-
21	84.1	76.1	77.9
22	79.8	74.3	-
23	75.8	72.6	-
24	71.1	70.6	-
25	85.0	76.3	77.9
2	80.1	74.5	-
27	76.3	72.7	-
28	71.2	70.6	-

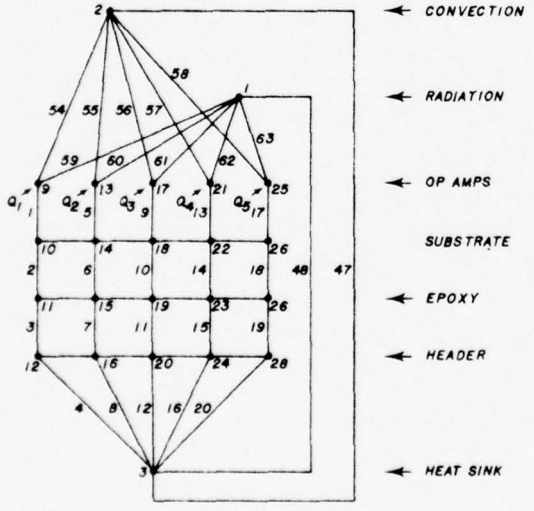

Fig. 11. Node diagram (no top on can).

lems. Of special interest was the placement of IC4 and IC5, the major power-dissipation nodes. The layout designer placed these chips on one end of the substrate separated by about one chip width in order to simplify his conductor routing. This was our chief candidate for a thermal problem. However, the thermal simulation and subsequent experimental results proved that a one-chip separation was sufficient [5].

The thermal-analysis results indicate that thermal simulation can be a valuable tool in the hybrid-circuit design process.

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Part 3

On the Use of Thermal Simulation in Hybrid Circuit Design

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ON THE USE OF THERMAL SIMULATION IN HYBRID CIRCUIT DESIGN

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ABSTRACT

This paper explores some of the problems in using thermal simulation as a design tool for the layout of hybrid microelectronic circuits. The paper begins with a general discussion of a proposed, interactive computer-aided design system for electrical design and topological layout of hybrid microelectronic circuits. Next, a thermal model for hybrid microcircuits developed in [1] is discussed. Preliminary device separation guidelines are developed. The thermal model is designed so that calculation of thermal parameters for the model may be done algorithmically by a general purpose computer. Application of the model to design automation is addressed. The model essentially serves as an interface between a computer-aided, interactive graphics layout system and a computer-aided thermal simulation, both of which are available now.

Experimental and theoretical results are contrasted.

INTRODUCTION

The analysis, design, and verification of a hybrid microelectronic circuit is a time-consuming process [1]. The electrical and thermal analysis, when done manually, becomes a critical item in the circuit development cycle since the electrical and thermal analysis procedures must be accomplished by a highly skilled engineer, whose time may be unavailable. Consequently there is a tendency to "short cut" these important steps in the circuit development cycle.

One solution to this dilemma is to employ computer-aided-design programs to accomplish both electrical analysis and thermal simulation. Figure 1 depicts a proposed system which employs interactive graphics techniques to decrease the time required for the circuit design and verification phases.

The concept of Figure 1 is described as follows:

1. A designer first enters his theoretical hybrid microelectronic network into the system using the interactive schematic program.

2. The schematic program outputs the circuit configuration and component values to the circuit analysis routine, which calculates the power dissipated (heat generated) at each circuit element, as well as other steady-state and transient circuit characteristics.

3. The results of circuit analysis are presented both tabularily and graphically to the designer on the CRT for circuit design verification. He may modify his circuit and return to circuit analysis until he is convinced that his hybrid microelectronic circuit theoretically satisfies his design criteria.

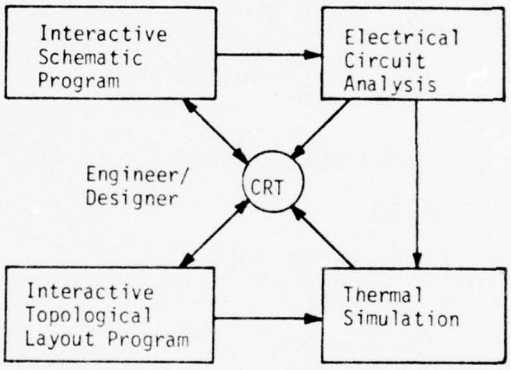

Figure 1. Interactive CAD Concept

4. Once a "good" electrical design is completed, the user may then employ the interactive topological program to generate the topological layout for his hybrid microcircuit. The layout shows the physical placement of each heat generating circuit element.

5. Topological information and material thermal parameters are used to calculate thermal input data for the thermal simulation routine. Using this topological data and the heat source data from the electrical circuit analysis routine, the thermal simulation routine determines the heat flow properties of the proposed circuit layout.

6. Thermal data is displayed to the user on the CRT for circuit layout verification. He may modify his layout and return to thermal analysis until he is convinced that the thermal properties of his layout are acceptable.

7. Once the designer is satisfied with the electrical and thermal properties of his circuit, he may use the interactive layout program to generate photo tools for actual microcircuit construction. These tools are usually generated on a high precision flat-bed plotter.

The unique feature of this CAD system is the inclusion of interactive thermal analysis. Computer programs exist that generate electrical schematics, that analyze transient and steady-state electrical properties of a circuit whose input is a schematic, that interactively layout the topology of a hybrid microcircuit, and that simulate the thermal properties of a circuit topology described in a nodal model notation. The weakest link in the system is the generation of a nodal model description of the circuit from its topological layout. The circuit layout is performed by a human designer, and hence the thermal nodal model must also be generated algorithmically as the topological layout takes form. A simplified nodal model, suitable for implementation in CAD systems, has been described in [1]. In what follows, a portion of this model that describes the thermal resistance from device to package is developed. Guidelines for designing circuits which will "fit" the model are also discussed.

CAD THERMAL CONSIDERATIONS

Basic Problems

From a thermal standpoint, the topological designer is confronted with basically two problems. These are:

1. Choice of size, materials and attaching techniques for the package, substrate and heat dissipating circuit elements, such that each dissipator has a sufficiently low thermal resistance to the ultimate heat sink. This assures device reliability. Knowledge of package mounting and heat removal means, must of course be considered in this choice.

2. Placement of heat dissipating circuit elements on the substrate, such that heat from one element does not appreciably raise the temperature of other dissipating elements, for a fixed header or package temperature. That is, the elements must be sufficiently separated so as to minimize thermal coupling.

It is assumed, that from a knowledge of total circuit heat dissipation, a suitable package and package heat removal means have been selected. The circuit size (number and type of elements) will of course be considered in package size selection. By the same token, it is assumed that substrate and substrate/header attach means have been selected in such a way to assure that with proper circuit element size, attach techniques and location, it will be feasible to obtain satisfactory thermal performance in the CAD phase. These parameters are entered into the thermal model of Cook, et.al., [1].

One problem remaining then, is to assure a sufficiently low thermal resistance, θ, from each heat dissipating circuit device to the package or header. The number of such devices as well as their dissipation is obtained from the circuit analysis block of the CAD system. Usually, many of these device dissipations are so small as to be inconsequential, leaving only a few devices of importance. For the remaining devices, certain choices must be made on an individual basis:

1. Area of thick film resistors
2. Size of IC or discrete transistor chips
3. Size and construction of any chip resistors
4. The bonding or attach technique of all chips to the substrate.

The thermal resistance of these devices to the package can often be computed by thermal simulation using an approximate spreading resistance model outlined by Harper [2]. This model gives conservative or slightly high values of thermal resistance. The model cannot be used for beam-lead or flip chip mountings, but authors such as Shamash, et.al., [3], discuss these cases with approximate results. The appropriate dimensions and other parameters are also entered into the thermal model.

The thermal conductance (reciprocal of thermal resistance) from the device heat generating region to the package or header will be designated as G, with units of watts/°C. The next section will show an example of the computation of G for actual devices using the spreading resistance model.

A second problem remaining is the placement of more than one heat generating device on the substrate. If they are spaced too closely, they will interact thermally with higher device temperatures than if they were isolated by themselves. If they are spaced too far apart, then metalization routing problems may become severe if not impossible. An example would be a power amplifier with two transistor chips in its output stange. Later in this paper, a relatively simple and reasonably accurate criterion is established to determine how far devices should be separated to provide reasonable thermal isolation. It will be found that relatively close spacing can be tolerated in most cases. If the designer uses these rules, he will obtain accurate results from the thermal simulation program of the CAD system.

Individual Device Thermal Conductance

The spreading resistance model [2] is illustrated in Figure 2. Heat flows through the layer of thickness d, entering the top through an area of dimensions a by b (a > b). The model assumes

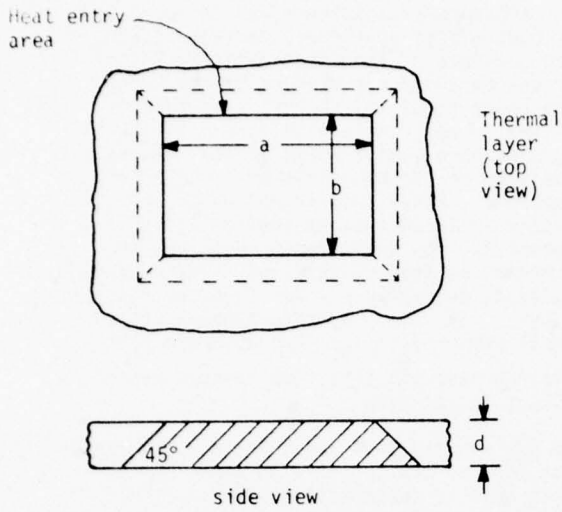

Figure 2. Spreading Resistance Model

a heat flow spread of 45° so that the heat exits the bottom of the layer through an area of dimensions a+2d by b+2d. The thermal resistance through the layer is given by

$$\theta_d = \frac{1}{2k(a-b)} \ln \left[\frac{a}{b} \cdot \frac{b+2d}{a+2d}\right] \qquad (1)$$

where k is the thermal conductivity of the layer. If the heat entry area is square (b=a), the thermal resistance is given by

$$\theta_d = \frac{d}{k(a^2+2ad)} \qquad (2)$$

The spreading resistance model is now applied to a transistor chip, eutectically bonded to an alumina substrate, which in turn is bonded by conductive epoxy to a Kovar header. This is illustrated in Figure 3. The appropriate parameters are assumed to be:

Chip θ_c=1°C/W (junction to bonding base)

a=100 mils b=90 mils

$T_{J_{max}}$=100°C (high reliability)

Substrate thickness=s=25 mils

$k_s=7.2\times10^{-4}$ W/mil-°C at 40°C [5]

$=6.2\times10^{-4}$ W/mil-°C at 100°C

Epoxy thickness=e=5 mils

$k_e=2\times10^{-5}$ W/mil-°C

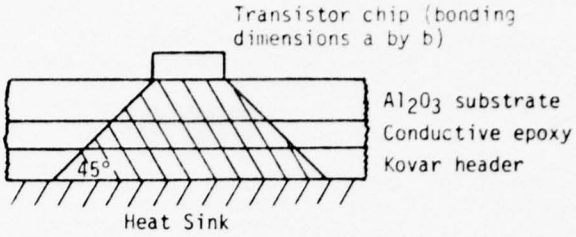

Figure 3. Chip Thermal Conductance by Spreading Resistance Model

Kovar Header thickness=h=30 mils

$k_h=4\times10^{-4}$ W/mil-°C

Heat Sink maintained at T_s=40°C

From Equation (1), the thermal resistance of the substrate layer is

$$\theta_s = 2.93 \text{ °C/W}$$

where the thermal conductivity for 100°C is used, since this represents approximately the top substrate surface temperature below the chip, when it is operated at $T_{J_{max}}$. For the thermal resistance calculation through the epoxy, the heat entrance area is increased to a+2s by b+2s. For the header it is increased to a+2s+2e by b+2s+2e. Equation (1) gives

$$\theta_e = 11.1 \text{ °C/W} \quad \text{epoxy layer}$$

$$\theta_h = 2.3 \text{ °C/W} \quad \text{header}$$

The total thermal resistance is

$$\theta = \theta_c + \theta_s + \theta_e + \theta_h = 17.3°C/W$$

and

$$G = \text{thermal conductance} = \frac{1}{\theta} = 0.058 \text{ W/°C}$$

The maximum power the chip should dissipate is

$$P_{max} = (T_{J_{max}} - T_0)G = 3.48W$$

This assumes that other dissipating devices on the substrate have negligible thermal coupling to the chip.

Thermal Coupling

Once it is assured that sufficient thermal conductance exists between the dissipating device and the heat sink, it is necessary to assure that devices are not placed so close as to cause excessive temperatures due to mutual heating. An alternative would be to allow appreciable coupling at the expense of maximum device power dissipations. It will be shown, however, that high dissipating device densities can be achieved with small to moderate coupling on many substrate-header configurations in common use. A criterion for dissipating device separation is developed, which is necessary for the simplified thermal simulation model of [1] to give reliable results.

It will be assumed that the product of thermal conductivity times thickness for the substrate is much larger than for the substrate bonding layer, such as epoxy. This is certainly true for the commonly used alumina-epoxy system examined in the previous section. Lateral heat flow will then be confined essentially to the substrate, and this heat flow will cause substrate surface temperatures rises away from the dissipating device. This temperature distribution will now be considered.

A square heat dissipating device with sides of length a, is located on top of the substrate as shown in Figure 4. A grid of equal area squares is formed. The mid-layer substrate temperature

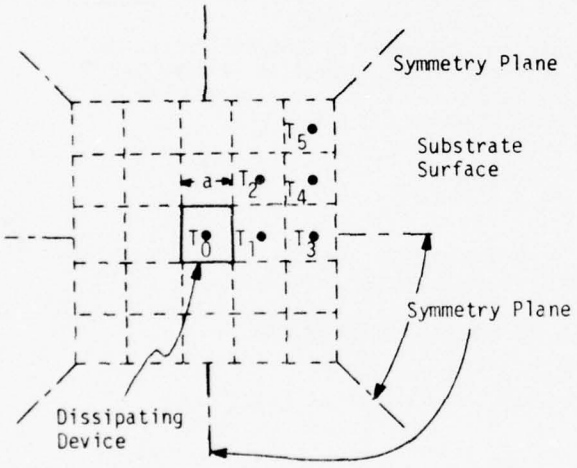

Figure 4. Substrate Temperature Distribution Around a Dissipating Device

below the device is T_0. T_1, T_2, T_3, T_4 and T_5 are the mid-layer temperatures within the appropriate squares of the grid. These latter temperatures are also essentially the surface temperatures of the substrate, since this surface is adiabatic. That is, no heat flows through the top substrate surface except under the device itself. This assumes negligible convection and radiation to the package, which is the case with enclosed circuits.

The temperatures, T_1 through T_5, are approximately the temperature rise another device would experience, when placed on the appropriate square, due to the presence of the first device. To this rise must be added the product of the second device power times its thermal resistance to the heat sink. The principle of superposition is being used here, which holds if the thermal conductivities of the materials are independent of temperature. While this is not quite true, it must be remembered that we are developing a criterion for low to moderate coupling, which if met, minimizes this restriction. The criterion, then, is to determine how far from the dissipating device will the substrate temperature rise be small compared to T_0. For accurate thermal simulation results, this rise is recommended to be 15% of T_0, or less.

It is now assumed that the substrate extends only to the edge of the grid. This approximation will tend to lead to conservative results. That is, higher than actual temperatures for T_1 through T_5. Temperaturewise, planes of symmetry exist as shown in Figure 4. Temperatures on one side of the plane are imaged on the other side. Therefore only one-eighth of the configuration needs to be considered. The lateral conductances connecting these nodes are shown in Figure 5. This conductance G_s is the conductance between adjacent temperature nodes within the substrate, and is given by

$$G_s = \frac{\text{(conductivity) x (cross-sectional area)}}{\text{length of path}} = \frac{k_s sa}{a} = k_s s \qquad (3)$$

where s is the substrate thickness. The lower two conductances are halved, since the plane of symmetry cuts them in two along their length.

Conductances also extend from each temperature node, through the layers to the heat sink. Their cross-sectional area is the area of each grid square, a^2. Their value is given by

$$G_v = \frac{1}{\theta_s'/2 + \theta_e' + \theta_h'} \qquad (4)$$

where $\theta_s' = \dfrac{s}{k_s a^2}$

$\theta_c' = \dfrac{e}{k_e a^2}$,

$\theta_h' = \dfrac{h}{k_h a^2}$

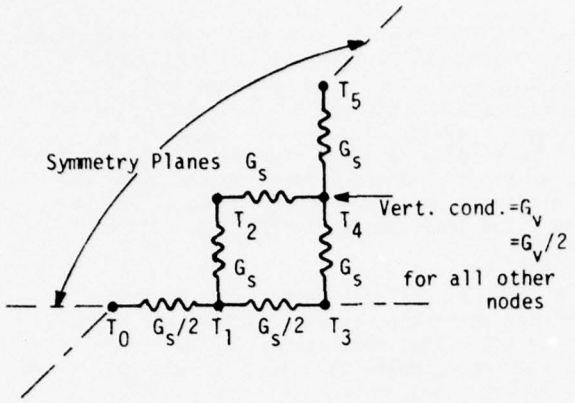

Figure 5. Conductance Pattern Near Dissipating Device

The θ_s term in the denominator of (4) is divided by 2 since the temperature nodes are in the middle of the substrate. Except for the node corresponding to T_4, the vertical conductances are also halved since a plane of symmetry cuts them along their length.

The temperature T_0 is assumed known. T_0 through T_5 are treated as the temperature rises above the sink temperature. Writing heat flow equations for the five nodes corresponding to temperatures T_1 through T_5 gives

$$\left(\frac{G_v}{2} + 2G_s\right)T_1 - G_sT_2 - \frac{G_s}{2}T_3 = \frac{G_s}{2}T_0$$

$$-G_sT_1 + \left(\frac{G_v}{2} + 2G_s\right)T_2 - G_sT_4 = 0$$

$$-\frac{G_s}{2}T_1 + \left(\frac{G_v}{2} + \frac{3}{2}G_s\right)T_3 - G_sT_4 = 0 \qquad (5)$$

$$-G_sT_2 - G_sT_3 + (G_v + 3G_s)T_4 - G_sT_5 = 0$$

$$-G_sT_4 + \left(\frac{G_v}{2} + G_s\right)T_5 = 0$$

A conductance ratio r is defined as G_v/G_s and is substituted into Equation (5). Solution of this system of equations results in Equations (6).

$$\frac{T_1}{T_0} = \frac{r^4 + 12r^3 + 47r^2 + 66r + 20}{r^5 + 16r^4 + 90r^3 + 213r^2 + 186r + 20}$$

$$\frac{T_2}{T_0} = \frac{r^2 + 7r + 13}{3r + 10} \cdot \frac{T_1}{T_0} - \frac{r + 3}{3r + 10}$$

$$\frac{T_3}{T_0} = -2\frac{T_2}{T_0} + (r + 4)\frac{T_1}{T_0} - 1 \qquad (6)$$

$$\frac{T_4}{T_0} = \frac{r + 3}{2} \cdot \frac{T_3}{T_0} - \frac{1}{2} \cdot \frac{T_1}{T_0}$$

$$\frac{T_5}{T_0} = \frac{2}{r + 2} \cdot \frac{T_4}{T_0}$$

This is shown in tabular form by Table 1.

DESIGN EXAMPLE

Returning to the transistor chip configuration of a previous section, we obtain from equation (3)

$$G_s = k_s s = (7.2 \times 10^{-4})(25) = 1.8 \times 10^{-2}\ W/°C$$

$r = G_v/G_s$	T_1/T_0 d = a	T_2/T_0 d = 1.4a	T_3/T_0 d = 2a	T_4/T_0 d = 2.3a	T_5/T_0 d = 2.8a
0.3	0.45	0.33	0.29	0.25	0.22
0.5	0.4	0.27	0.24	0.22	0.17
0.8	0.31	0.18	0.15	0.13	0.09
1	0.27	0.14	0.11	0.07	0.05
1.3	0.25	0.11	0.08	0.05	0.03
2	0.2	0.08	0.05	0.03	0.01
3	0.16	0.05	0.03	0.015	0.006
5	0.13	0.03	0.016	0.006	0.0016
7	0.095	0.018	0.01	0.003	0.0006

Table 1. Temperature Ratios versus Conductance Ratio

where the substrate thermal conductivity for 40°C was used. This is done since most of the substrate surface being considered here is not under the device and is probably closer in temperature to the heat sink than to T_0. This will give conservative results as far as coupling is concerned.

The conductance through the layers to the heat sink is computed by assuming a square device of sides $\sqrt{(100)(90)} = 94.8$ mils, for which equation (4) gives

$$G_v = \frac{(94.8)^2}{\frac{25}{2(7.2\times10^{-4})} + \frac{5}{2\times10^{-5}} + \frac{30}{4\times10^{-4}}} =$$

$$2.63 \times 10^{-2} \text{ W/°C}$$

The conductance ratio is then

$$r = \frac{G_v}{G_s} = 1.46 \simeq 1.5$$

It is decided that other devices should be placed far enough away so that the coupling temperature ratio is less than 5%, which assures almost complete thermal isolation. From Table 1, we see that a second device placed at the location of T_4 achieves this result. That is the distance d, (center to center), of the devices should be 2.3a, where a = 94.8 mills, the mean chip dimension. This does not mean the devices have to line up vertically or horizontally. Figure 6 shows several possibilities for this particular example. It should be mentioned that the above computation of G_v should be made for the larger of the two devices, with the distance d based upon the mean dimension of the larger device and Table 1.

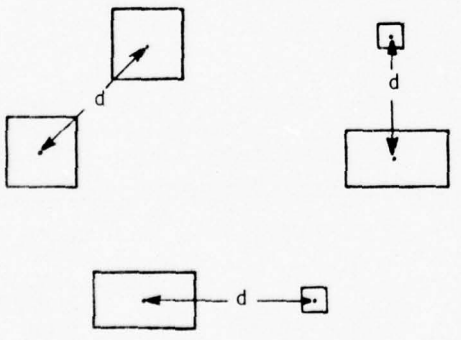

Figure 6. Device Separation for Negligible Thermal Coupling (d ≥ 2a where a is the mean dimension of the larger device)

EXPERIMENTAL VERIFICATION OF COUPLING RATIOS

A cermet paste resistor was formed on a substrate/header combination, identical to that used for the example problem. The resistor is 50 by 100 mils and was powered at a level of 3.67 W. The mean resistor dimension is therefore $a = \sqrt{50 \times 100} = 71$ mils. Three small temperature sensor diodes [5] are located on the substrate at distances corresponding to 0.71a, 2.1a and 2.8a. The lower header surface was held at 26°C.

By a thermocouple measurement, the maximum temperature on the resistor surface was found to be 109.6°C. The temperature, in the middle of the substrate, below the resistor, was calculated to be $109.6° - \frac{\theta_s}{2}(3.67W) = 101.2°C$. This is a difference of $T_0 = 75.2°C$ from the header temperature. While determination of T_0 in this way is quasi-experimental, there is no convenient way to directly measure the mid-substrate temperature. The result should be accurate to within a couple of degrees.

The conductance ratio is readily calculated to be $r = 0.83 \simeq 0.8$. Figure 7 shows a curve plotted through the points of Table 1, corresponding to this value of r. The temperature ratios, as measured at the diode sensors are also shown.

In general, experimental results using other device configurations probably cannot be expected to agree as closely. It is recommended that the table be used as a guide. That is, for an acceptably low coupling ratio, such as 15%, the actual separation distance should be at least that given by the table.

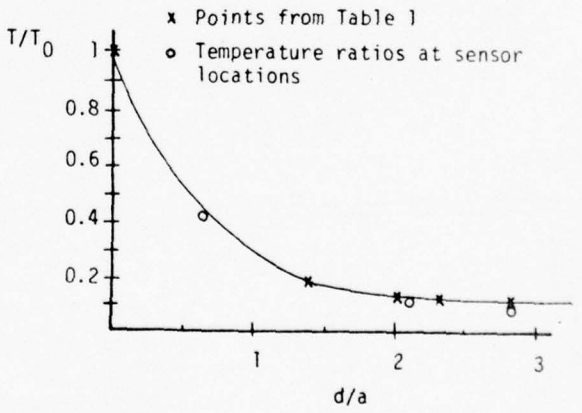

Figure 7. Thermal Coupling Ratios, Experimental versus Calculated

CONCLUSIONS

This paper has described at the conceptual level a proposed interactive computer-aided-design procedure to assist the designer of complex hybrid microelectronic circuits to perform electrical design, topological layout, and thermal simulation. The major focus of the paper has been on a simplified thermal nodal model for the hybrid circuits. Theoretical and experimental justification for portions of the model in [1] have been presented in this paper. Design guidelines for device separation have been presented to aid the hybrid designer in his topological layout. The adherence to these guidelines helps insure that the simplified thermal model of [1] will give realistic results.

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Part 4

Thermal Analysis and Measurement of Hybrid Microcircuits

Prepared for

U. S. Army Missile Command

Redstone Arsenal, Alabama

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FOREWORD

This is a technical report of the progress on thermal analysis and measurement of hybrid microelectronic circuits, conducted by the Electrical Engineering Department of Auburn University for the U.S. Army Missile Command at Huntsville, Alabama. The report is primarily concerned with thermal analytical modeling and experimental verification of power dissipating circuit devices on hybrid systems.

I. INTRODUCTION

A. Objectives

The primary objective is to develop a thermal modeling procedure to characterize heat dissipating devices on a hybrid microcircuit and to verify these models with experimental measurement. The models are to be such, that it would be feasible to incorporate them as thermal computer-aided-design tools. In addition, thermal measurement techniques are to be developed and a preliminary evaluation made. Results, both analytical and experimental, are then to be used for outlining certain thermal design, layout and construction criteria for effective heat removal and temperature control.

B. Investigative Approaches

The problem addressed is that of determining the thermal resistance from the heat generating region of hybrid circuit devices to the package header. This resistance, once determined, allows a rapid calculation of maximum device heat dissipation for a given peak device temperature. Package (particularly header) temperature is also assumed known. Determination of package temperature usually requires an external heat flow investigation. However except for package size, this is essentially independent of the hybrid circuit layout and design, and is not considered in this investigation. The reader is referred to the literature [1,2,3,4] for treatments of this problem.

Heat flows by conduction from the heat generating regions of individual devices to the package header. Internal radiation, convection, or conduction through the enclosed nitrogen filled space is negligible, as concluded by Pogson [5] and Daniels [6]. Conductive flow from the devices through the substrate and other layers to the header is therefore the basis fo this study.

1. Analytical Thermal Studies

The application of well known conductive heat flow laws to microelectronic circuits has been approached in many ways, with varying degrees of success. Most approaches can be classified as one or a combination of the following:

a. Analytic solutions of the three-dimensional partial differential equations for static heat flow.

b. Use of approximate physical models for three-dimensional heat flow.

c. Graphical techniques.

d. Numerical techniques for approximate solution of the exact three-dimensional partial differential equation formulation for the boundary-value problem.

Analytic solutions, if obtainable, give high accuracy. This requires however, idealized shapes and boundary conditions, as well as low geometrical complexity. Various transforms and/or eigen-function expansions are usually used [7,8,9]. The complexity of a total hybrid structure generally rules out these methods. Likewise, boundary conditions are rarely ideal, or even approximately so.

Approximate physical models, using such concepts as shape factors and spreading resistance [10] allow calculation of at least parts of the overall thermal circuit by simple formulas. These models have low accuracy because temperature is assumed to vary as a function of one independent spatial variable only. This is true for only a few idealized geometries, and even if applied in piecemeal fashion to a complete hybrid module, would give low accuracy results. However, for a preliminary quick estimate of thermal resistance, these methods may have some merit.

Some graphical methods, mainly that of curvilinear squares [11], do exist. These are limited to two-dimensional heat flow, and since their application requires a certain degree of "art" talent, they are not apparently applicable to computer solution. Also, where layers of different media exist, they are extremely difficult to apply.

Numerical techniques require the subdivision of the physical model into many "small" regions. Each region, containing a node, is separated from each adjacent region by a simply calculated thermal conductance. The problem basically then is to solve a system of N equations in N unknowns, where N is a large number. Dusinberry [12] was one of the first to treat this problem in some detail. Only since application of large-scale computer systems, has it been practical to employ numerical techniques to complex geometries.

Analytical studies for this work do employ numerical solution of the appropriate partial-differential equation and boundary conditions by use of the finite difference formulation of these equations. This method, along with hybrid circuit ramifications, is discussed at length by Ruwe and Slagh [4].

2. Experimental Thermal Studies

Experimental determination of the thermal resistances for devices requires temperature and power dissipation measurement. The measurement, either directly or indirectly, of the heat generating region temperature of the circuit device presents the most difficulty. The junction region of a transistor is a typical example.

The devices considered are electronic circuit devices that dissipate heat power to a heat sink, which is usually a header or some part of a package. Several examples are:

a. Discrete transistors

b. Packaged integrated circuits (IC's)

c. Transistor or IC chips mounted or bonded to a substrate, which in turn is bonded to a header

d. Thick or thin film resistors on substrate/header

e. Chip resistors on substrate/header

Where power dissipation of these devices is significant, it is important to know the maximum temperature within the device that will be reached, for a given header/package temperature. This temperature may be readily calculated if the thermal resistance, θ_{JC}, of the device is known. That is:

$$T_J = T_C + P\theta_{JC}$$

where

T_J is the temperature of the heat dissipating region of the device.

T_C is the sink, header or package temperature.

P is the device heat dissipation in watts.

This thermal resistance is illustrated in Figure 1.

While device power, P, and sink temperature, T_C, may be easily and accurately measured, the actual heat generating region temperature, T_J, cannot easily be directly measured. Some currently used procedures are:

a. Infrared measurement [13].

b. Variation of some temperature dependent parameter of the device such as junction voltage or current gain of a transistor. Pulsed techniques are usually used [14].

c. Liquid crystal [13].

These procedures suffer many disadvantages. Infrared measurements require elaborate optical systems, and recording equipment. The surface must be treated to assure opaqueness and its emissivity must be known. Pulsed parameter measurement techniques also require extensive instrumentation and fail when device thermal time constants are of the same order of magnitude as electrical time constants; such as in the case of smaller devices. Liquid crystals are limited in temperature range and several solutions must be available. Solutions must be calibrated and are susceptible to contamination and coating thickness variations.

Thermocouple micro-probes were chosen for temperature measurement of heat generating regions; primarily because of their ease of use, and the minimal amount of instrumentation required. These probes measure surface temperature, which may differ from heat generating region

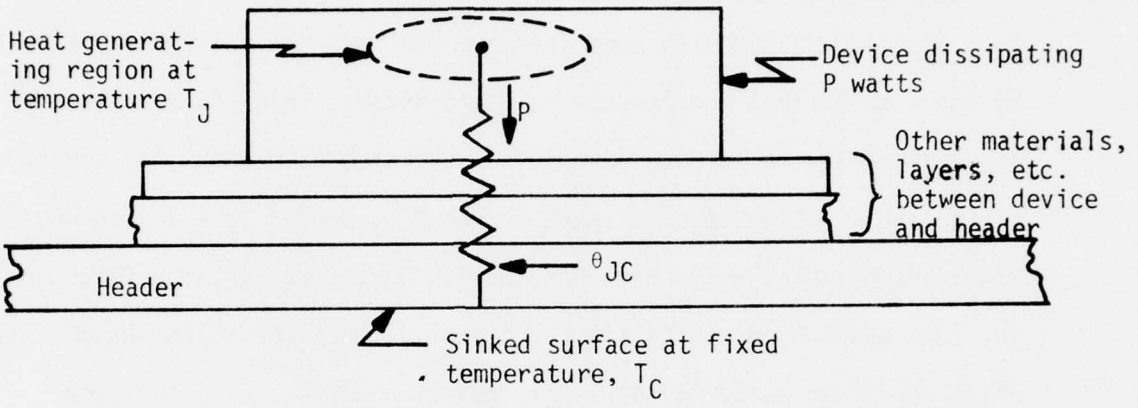

Figure 1. Device Thermal Resistance, θ_{JC}

temperature. A differential temperature measurement, varying header temperature and power dissipation such that the probe temperature remains fixed, removes this source of error. Sensor junctions and probes are used for substrate surface temperature measurement.

C. Test Circuit Modules

Hybrid test circuits were designed for experimental verification of the mathematical models used for transistors, thick film resistors and chip resistors. These were then fabricated at MICOM. All devices, along with junction sensors, were screened or bonded to a 1 inch square alumina substrate, which was epoxy bonded to the header of a flat pack. The test modules for thick film resistors, transistor chips and resistor chips are shown respectively in Figures 2, 3 and 4. Film resistor circuits also include straight and L-trimmed resistors to study the effect of uneven heat generation over the surface.

These units employ rather large devices for heat generation. It is felt that if mathematical models are verified for these, then the same type of models would be justified for any device size. Because of their size, thermal probing can be done on the device itself.

Structures were chosen to make maximum use of symmetry. This serves at least two purposes. First, the actual mathematical model formulation will be simplified, as well as requiring less computer time and memory. Though non-symmetric structures are usually encountered in practice, these can be modeled by the same techniques and will be valid provided the symmetric case has been verified experimentally.

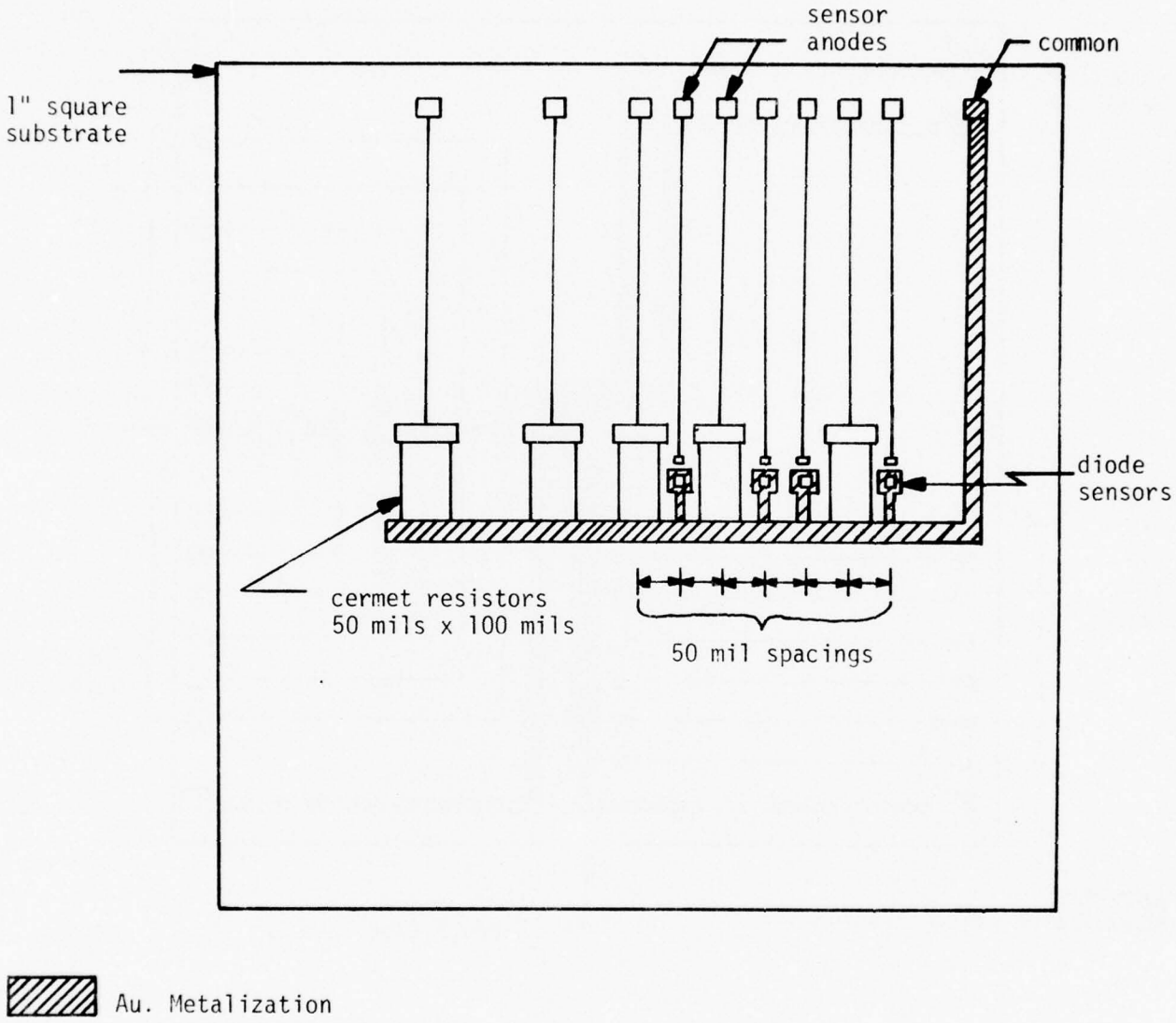

Figure 2. Thick Film Resistor Test Circuit.

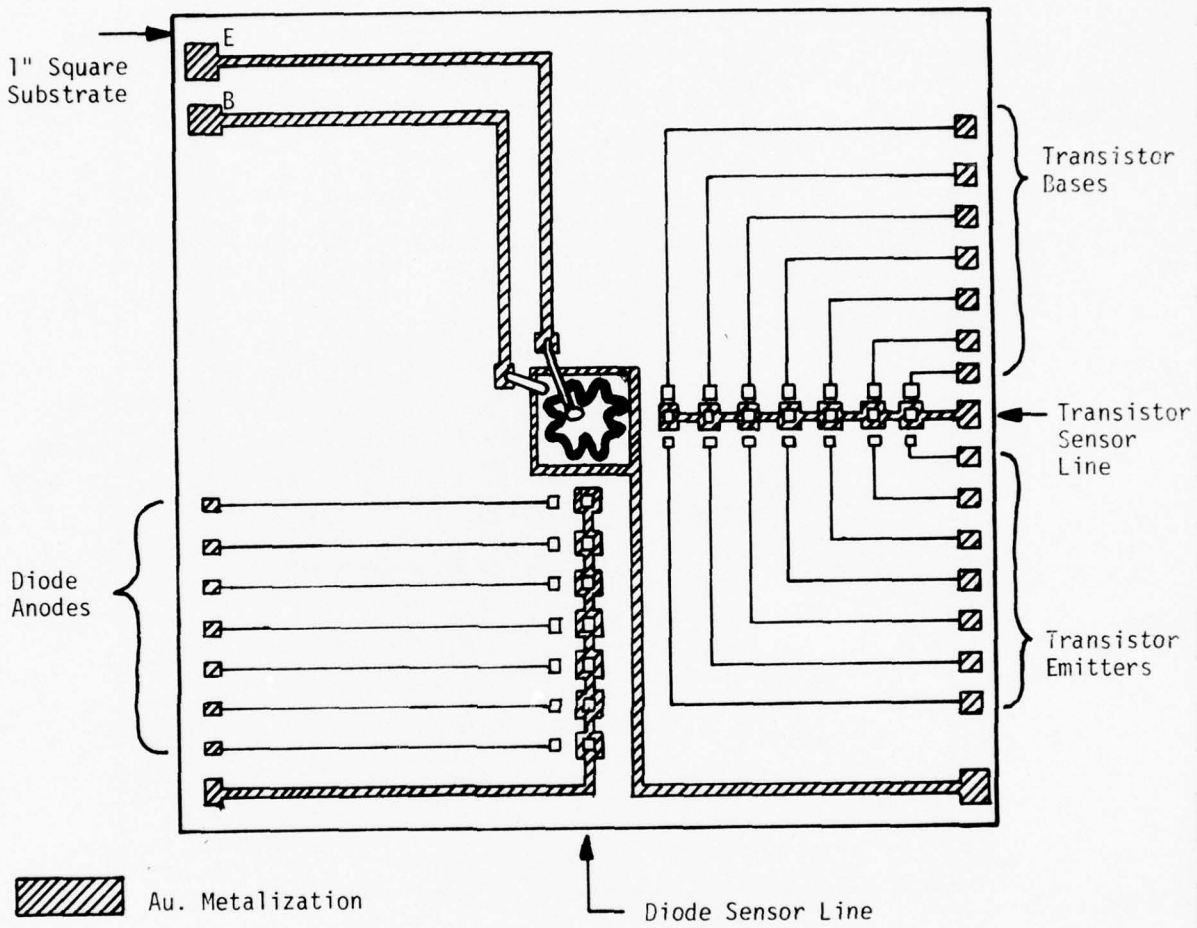

Figure 3. Chip Transistor Test Circuit

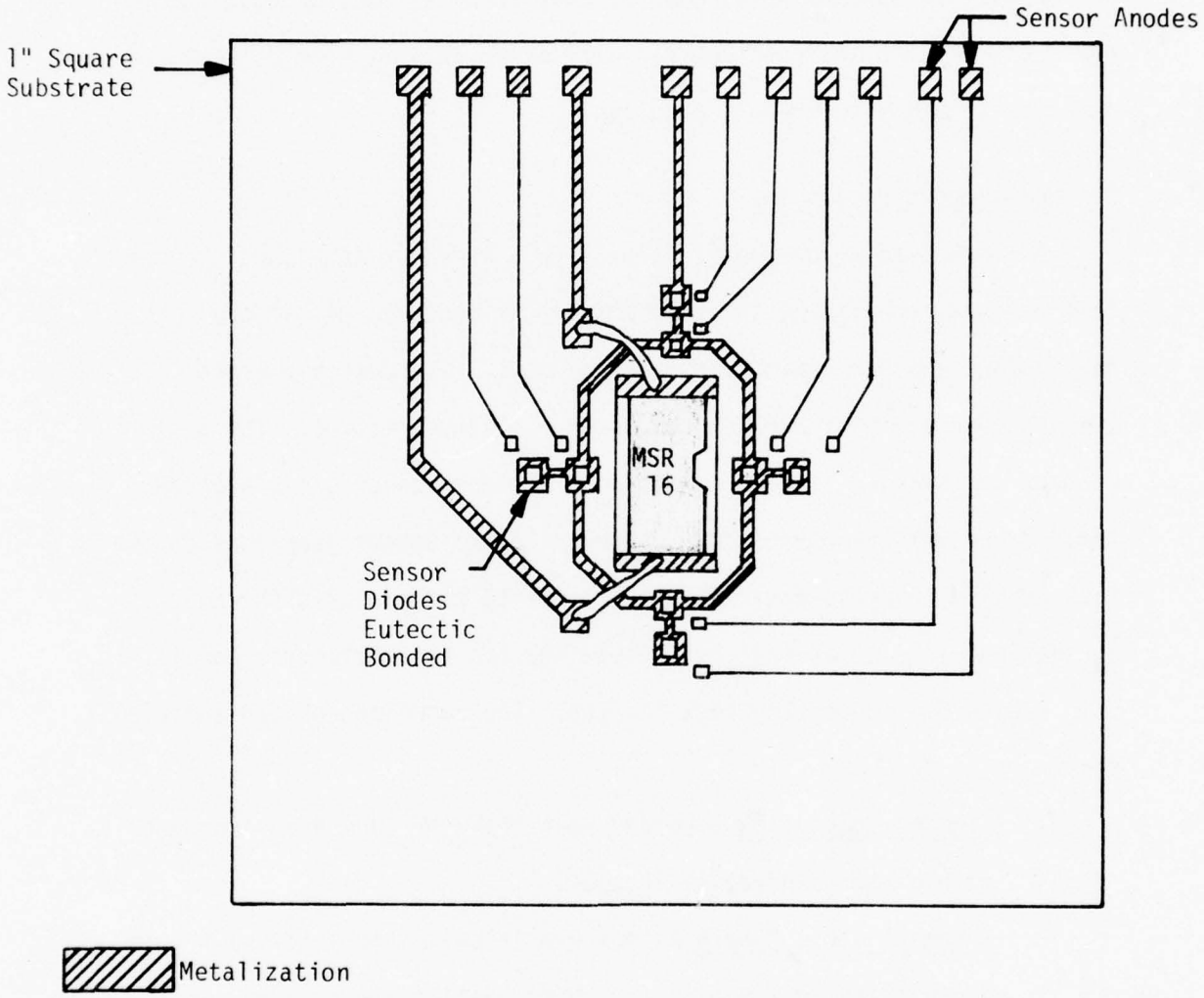

Figure 4. Chip Resistor Test Circuit

Second, this symmetry allows a cross-checking of different temperature measurement techniques, which employ junction sensors and thermocouple probes.

Substrate surface measurements, away from the heat generating device, will also indicate how far away other devices should be placed in order to minimize thermal coupling.

D. Measurement Facilities

A block diagram of the facility layout is shown in Figure 5. The test fixture, containing the test module, is enclosed within the temperature chamber, which can heat and cool. Thermocouple probe temperatures are monitored by thermometer instrumentation. The test chamber temperature is also monitored. A diode sensor calibrator and temperature measurement circuit connects to the sensor junctions on the test module. Power supplies furnish power to the sensors, the heat generating elements on the test module and the thermoelectric module.

Figure 6 pictures the test fixture. The functions of the individual parts are as follows:

1. Aluminum Heat Sink provides heat transfer to the environment within the temperature chamber.
2. Thermoelectric Module allows electrical control of the hybrid circuit header temperature. Both heating and cooling are possible, depending on current direction.
3. Copper Heat Spreader assures that the hybrid circuit header is maintained at a uniform temperature.

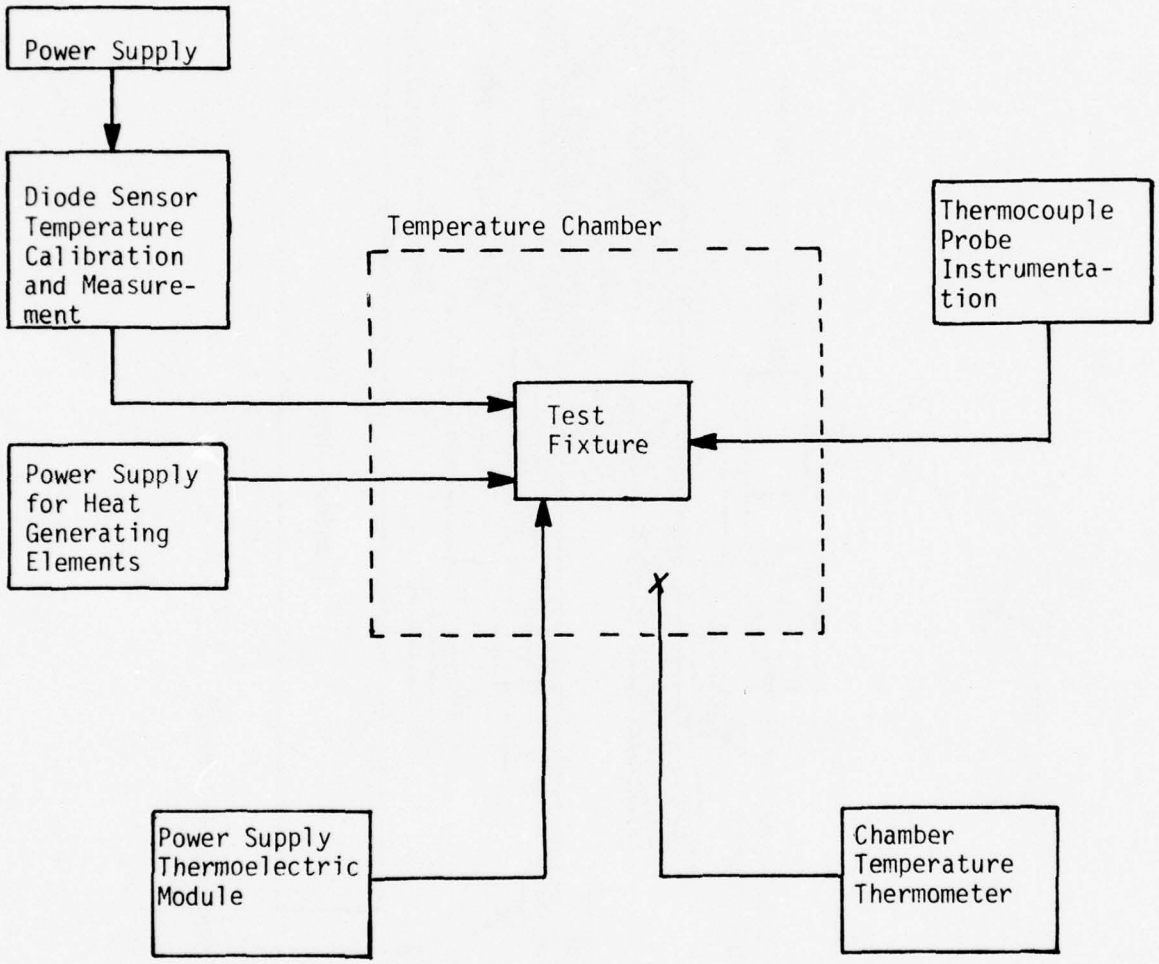

Figure 5. Measurement Facility Block Diagram.

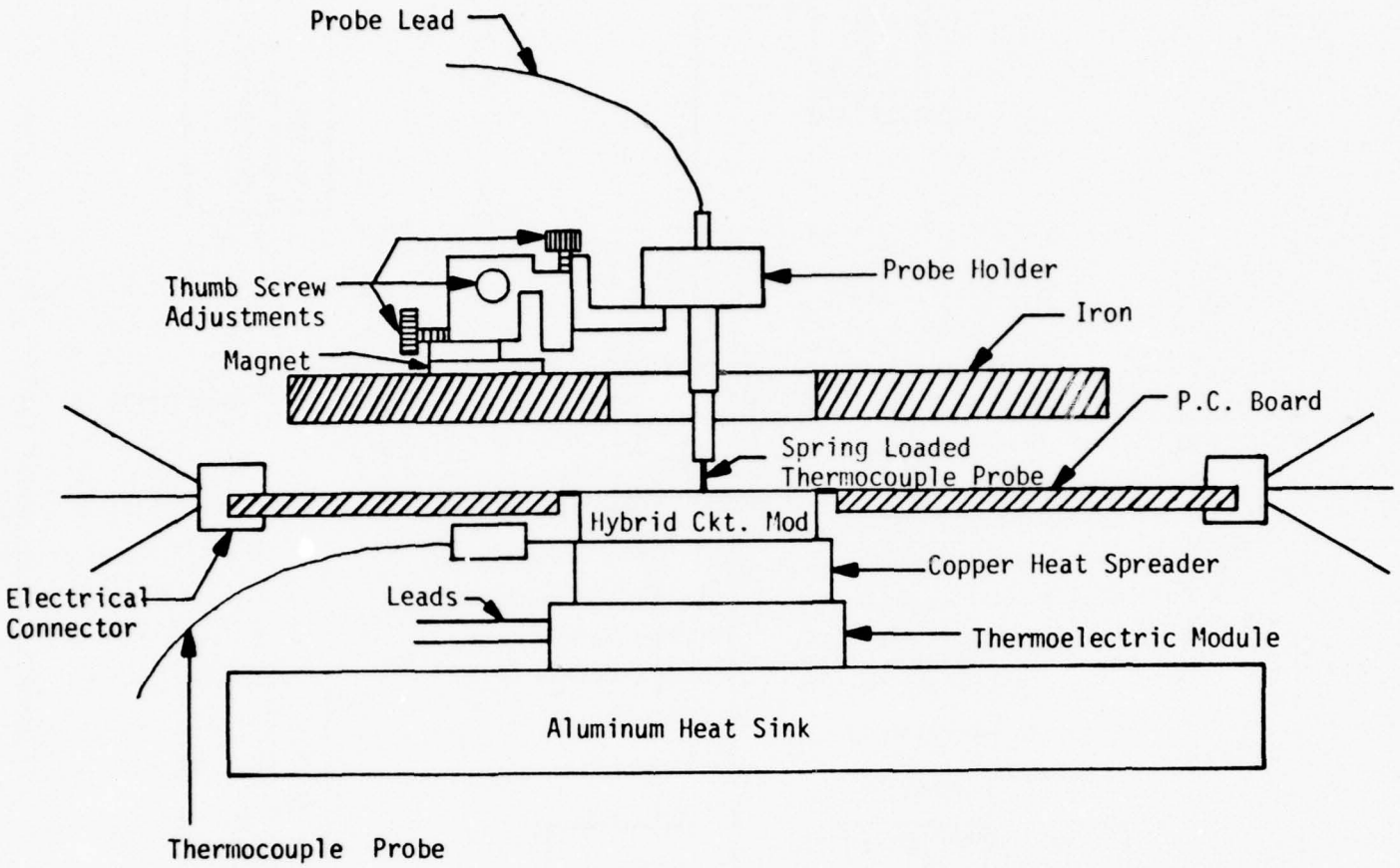

Figure 6. Hybrid Thermal Test Fixture.

4. Thermocouple Probe under Header monitors header temperature so that thermal resistances from heat sources to header, in the hybrid circuit, can be determined.
5. P.C. Board and Connectors provide electrical connection to heat sources in the hybrid circuit, as well as to sensor junctions. These sensors are calibrated and used for measurement with fixed forward current. They provide surface temperature measurements at various points on the substrate.
6. Spring Loaded Thermocouple Probe measures actual heat source (chips, resistors) temperature. Fixed probe pressure is assured for each measurement. The probe is 13 mils (0.013 in) in diameter. A differential temperature measurement cancels probe reading error. Provision is also made for a convection shield over the hybrid circuit (not shown).
7. Probe Holder and Positioner rests on and is held magnetically to an iron platform. The probe is accurately positioned and the pressure adjusted by micrometer thumb screw type adjustments.

A summary of the facility capabilities is listed below:

1. Independent header temperature control and monitoring.
2. Independent ambient (within chamber) temperature control and monitoring.
3. Substrate surface temperature measurement by junction sensors.
4. Peak temperature measurements on actual heat sources by probes.
5. Pressure and position adjustments for probes.
6. Hybrid test circuits on P.C. boards may be quickly changed.

II. THERMAL ANALYSIS TECHNIQUES

A. Model Formulation

The formulation of finite-difference models primarily involves three aspects. First is the designation of heat generating regions and the heat dissipation densities. Second, the nodal layout is assigned so that high node densities exist near the heat generating regions, and lower densities in more remote regions. Finally, thermal conductance values between nodes are calculated, based upon region thermal conductivities and conductance dimensions. Models were formulated for the thick film resistor test circuit (Figure 2) and the chip transistor test circuit (Figure 3).

1. Nodal Layout for Finite-Difference Solution

The nodal layouts for the thick film resistor and transistor test circuits are shown respectively in Figures 7 and 8. The procedure for this is described in detail by Ruwe and Slage [4, pp. 49-57]. Both epoxy and eutectic bonded transistor chips were modeled. Parameters are as follows:

a. Header (Kovar)
   30 mils thick
   1"x1" active area
   $k = 3.8 \times 10^{-4}$ W/mil-°C

b. Conductive Substrate Epoxy (Epotek H-74)
   5.5 mils thick (Fairly consistent for all units)
   1"x1" active area
   $k = 2.8 \times 10^{-5}$ W/mil-°C

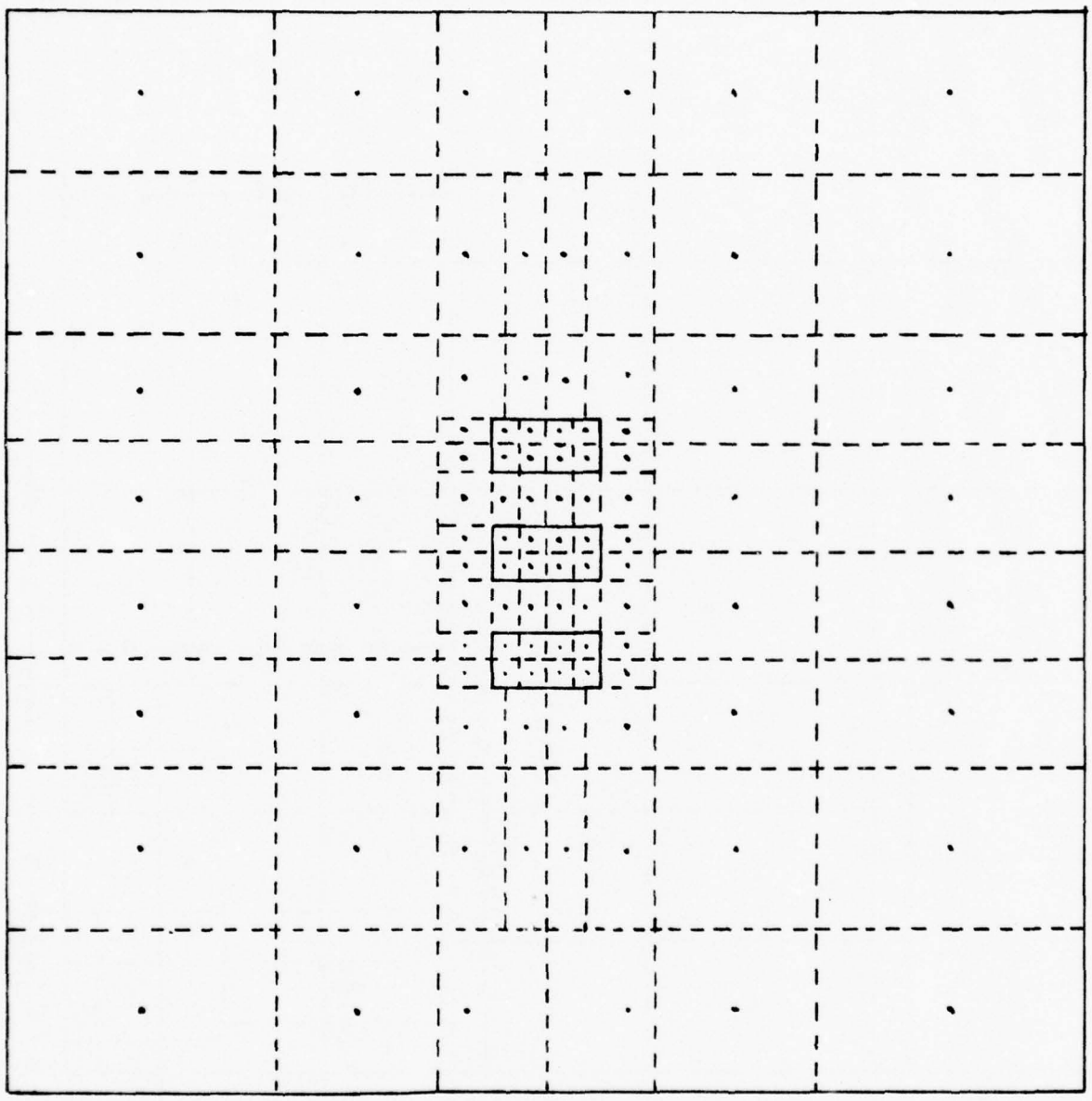

Figure 7. Nodal and Conductance Layout for Thick Film Resistor Test Circuit.

Dimensions are in units of 15 mils.

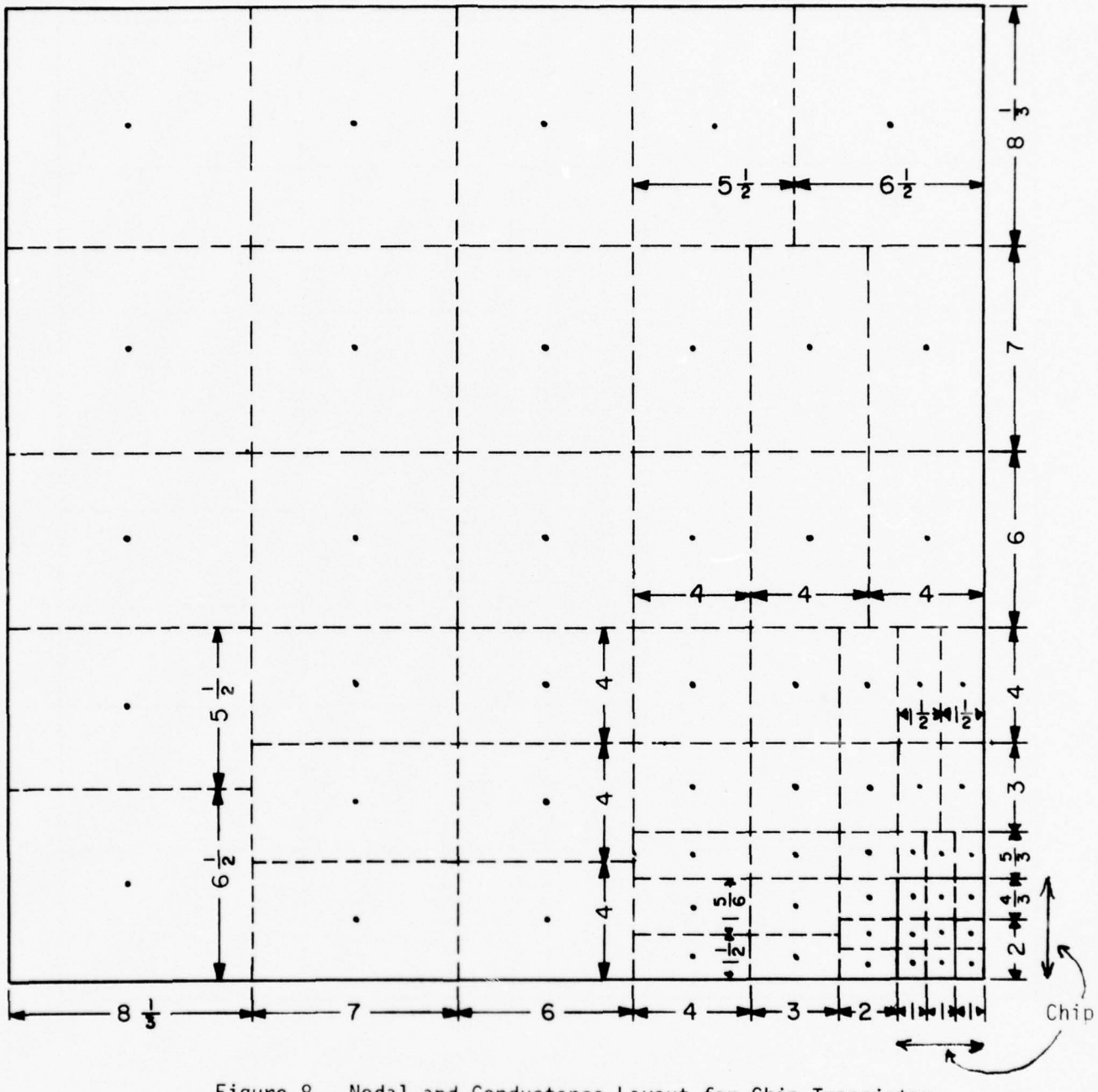

Figure 8. Nodal and Conductance Layout for Chip Transistor Test Circuit. One-fourth of Surface Shown.

c. Substrate (96% Alumina)
   25 mils thick
   1"x1" active area
   $k = 4.6 \times 10^{-4}$ W/mil-°C at 20°C
   $= 3.7 \times 10^{-4}$ W/mil-°C at 100°C

d. Cermet Paste Resistors
   50 x 100 mils
   300 ohms/square
   approximately 0.87 mils thick

e. Transistor Chip Epoxy (conductive)
   1 mil thick approximately
   100 x 90 mils active area
   $k = 4.8 \times 10^{-5}$ W/mil-°C

f. Transistor Chip
   8 mils thick
   100 x 90 mils
   $k = 2.44 \times 10^{-3}$ W/mil-°C (75°C)
   60 x 30 mils heat generating area

2. Heat Dissipation Distribution for Trimmed Resistors

Both straight and L trimmed resistors were investigated to determine the heat dissipation distribution. Unlike the untrimmed resistors, the surface current distribution is non-uniform. Figure 9 shows a trimmed resistor, with V_0 volts applied. The potential V and electric field $\bar{E}$ are represented by

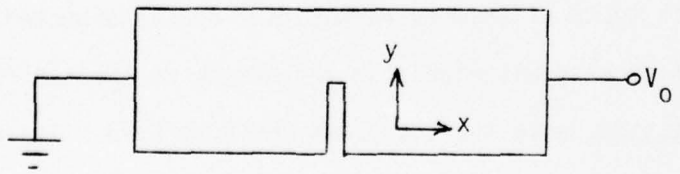

Figure 9. Trimmed Resistor Geometry.

$$V = V(x,y) \text{ volts}$$

$$\bar{E} = -\nabla V = -\frac{\partial V}{\partial x}\bar{a}_x - \frac{\partial V}{\partial y}\bar{a}_y \text{ volts/mil}$$

The surface current density, $\bar{J}$, is then

$$\bar{K} = \sigma\bar{E} = -\sigma\left[\frac{\partial V}{\partial x}\bar{a}_x + \frac{\partial V}{\partial y}\bar{a}_y\right] \text{ amps/mil}$$

where σ is the reciprocal of the sheet resistance in ohms/square. The heat power dissipation density is then given by

$$W_h = \bar{K} \cdot \bar{E} = \sigma\left[\left(\frac{\partial V}{\partial x}\right)^2 + \left(\frac{\partial V}{\partial y}\right)^2\right] \text{ watts/mil}^2$$

Determining the potential, $V(x,y)$, must be done by solution of Laplace's equation

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0$$

and application of appropriate boundary conditions at the ends of the resistor and along the edges including the "cut." A finite-difference procedure which is readily applied is described by Hayt [15]. This was done for both types of trimmed resistors. As was expected, the heat dissipation density was higher in the narrow restricted region of the resistors, and hence the hot spots would be here. The heat density distribution was incorporated into the model by inputting the appropriate heat power into the various resistor nodes (Figure 7).

B. Computer Solution Techniques

Obtaining the model node temperatures was effected by solving N equations in N unknowns by a standard computer program [4]. The device thermal resistance is then the ratio of the difference between the highest node temperature and the header temperature divided by the total device power dissipation.

The results are given is Section IV, where they are compared with experimental measurements.

III. EXPERIMENTAL MEASUREMENT

A. Sensor Diode Use and Calibration

Small diodes are located on the substrates of the test circuits to measure surface temperature. These diodes have the characteristic, that for fixed forward current, the junction voltage decreases about 2.5 mV per °C rise in temperature. A low fixed current (25μA) is used so that electrical heat generation is negligible.

The diodes are calibrated by placing the test circuit in the temperature chamber and varying temperature over the range of interest (20°C to 100°C). WIth the exception of the small fixed diode current, none of the devices on the circuit are powered. Diode voltage is calibrated against temperature. Typically, over the temperature range from 20°C to 100°C, the voltage will drop from about 510 mV to about 300 mV.

After calibration, the diodes may be used to measure substrate surface temperature, with the dissipating device under power. Diode locations are shown in Figures 10 through 14.

B. Probe Measurement Locations

Thermocouple probe temperature measurements were taken on the surface of the heat dissipating device. The measurement location is designated by the symbol, x. Generally this location is in the center of the device, except for the two trimmed resistors, where the measurement

was made in the center of the restricted cross-section. This is where maximum temperatures will occur. Only the center resistor of the screened resistor test circuit was powered.

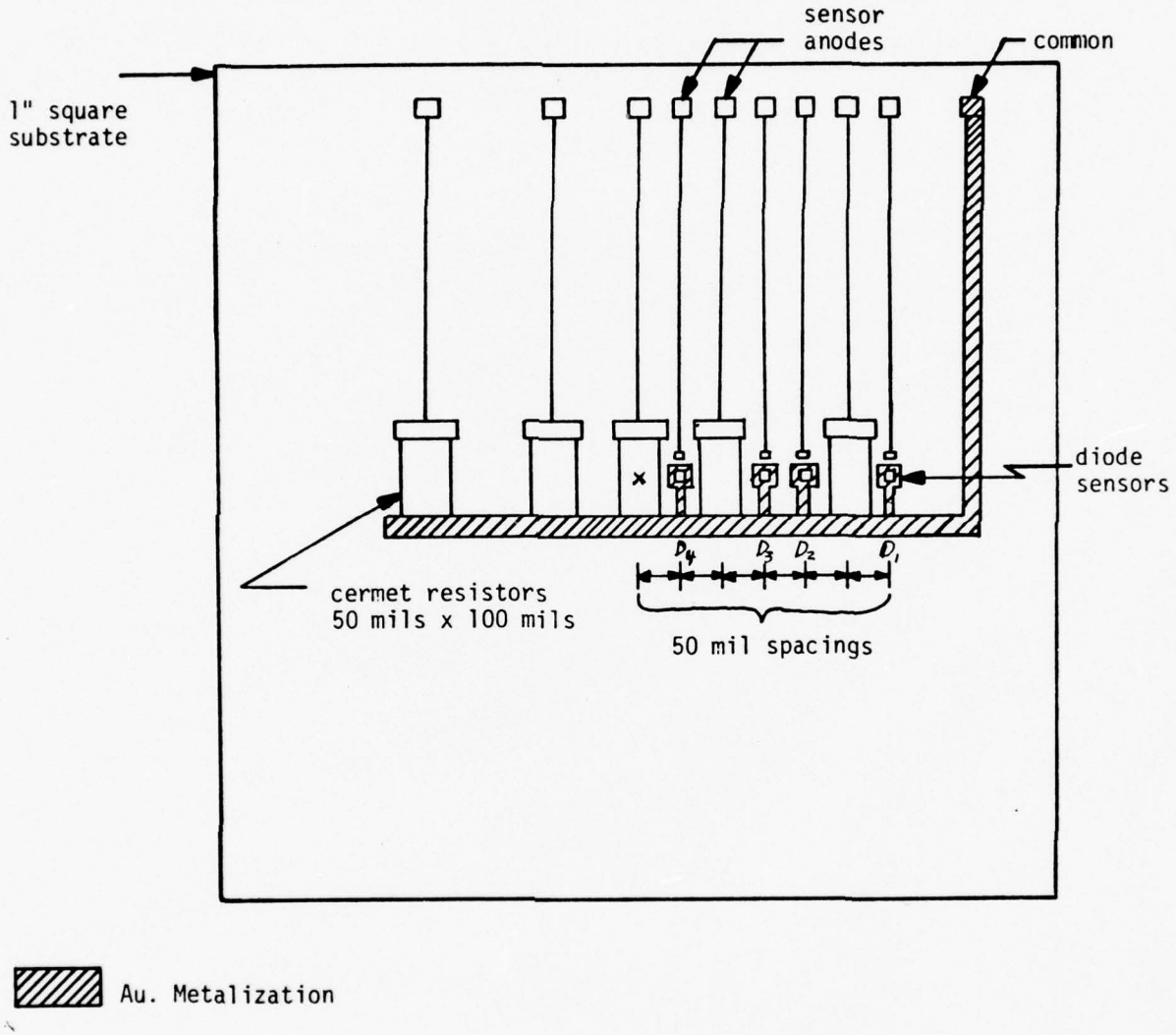

Figure 10. Un-Trimmed Resistor Test Circuit Measurement Points.

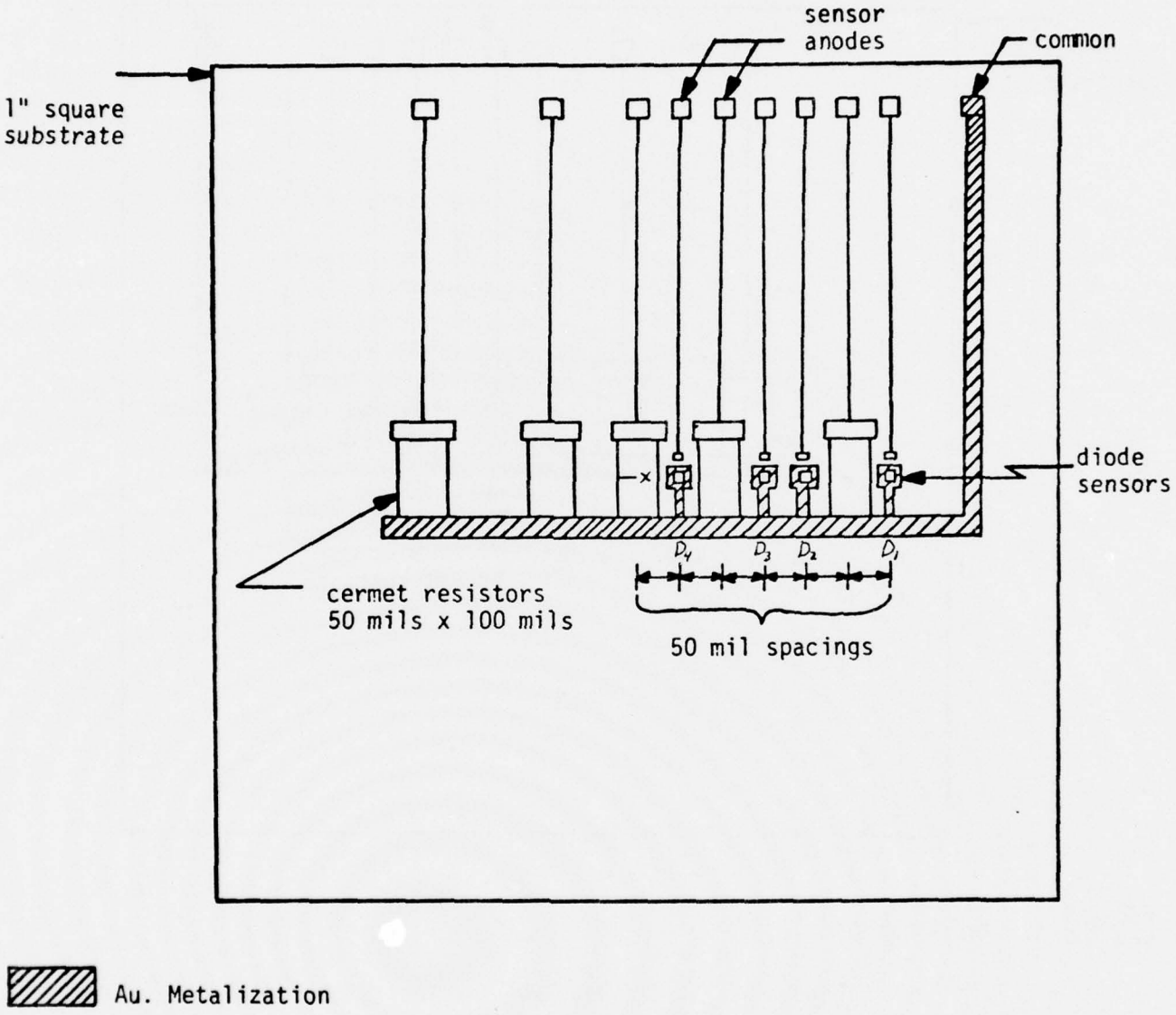

Figure 11. Straight-Trimmed Resistor Circuit Measurement Points.

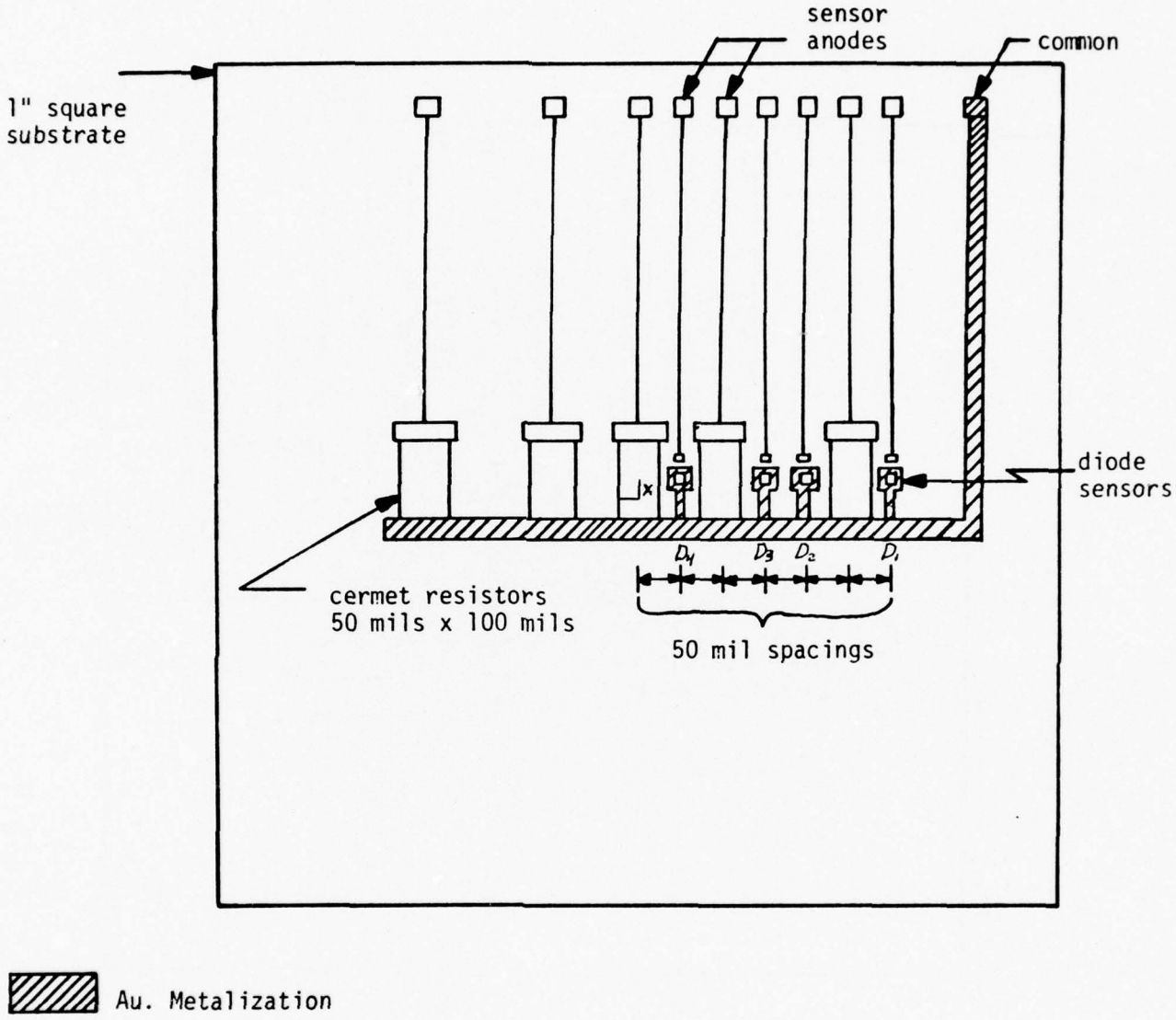

Figure 12. L-Trimmed Resistor Test Circuit Measurement Points.

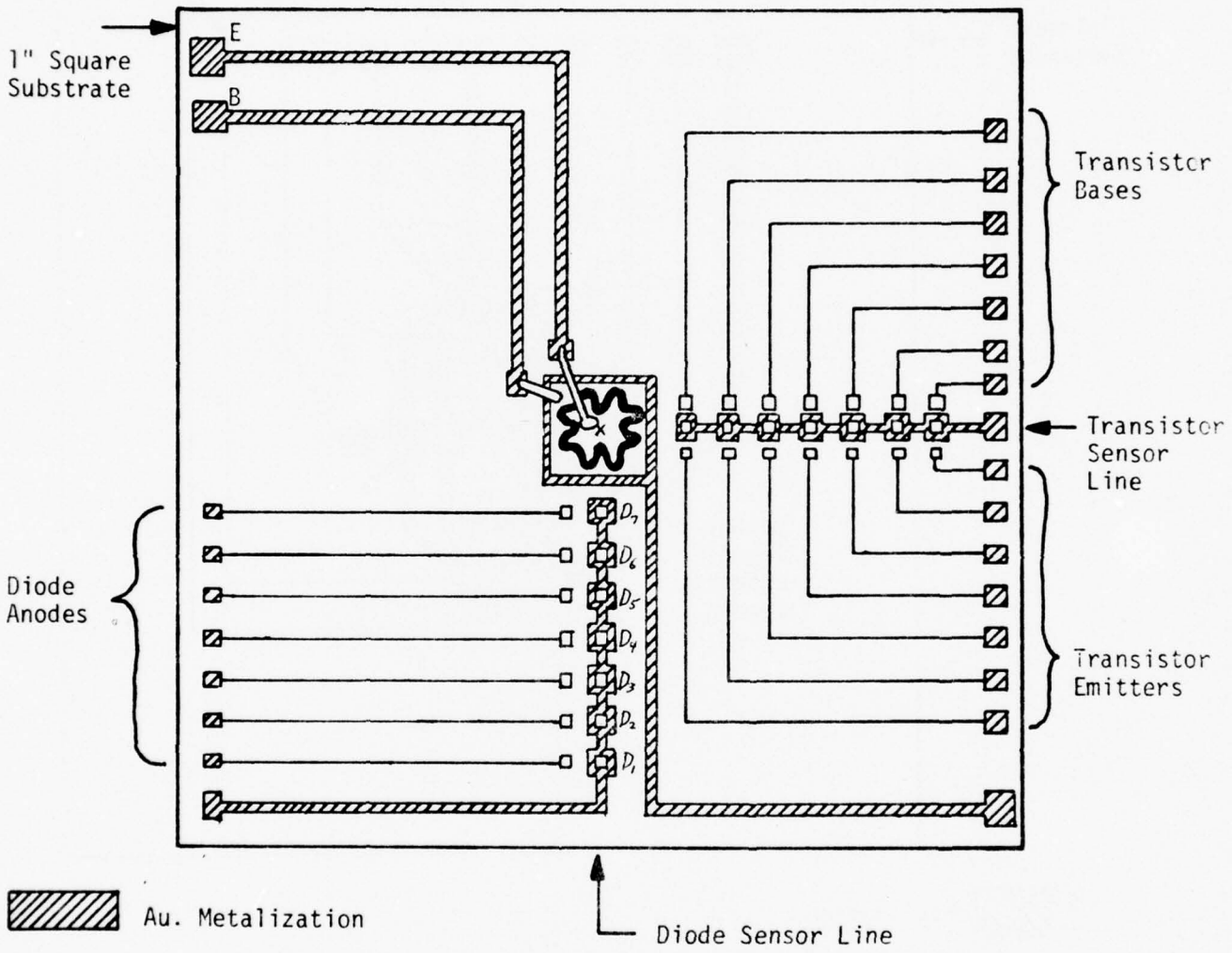

Figure 13. Chip Transistor Test Circuit
Measurement Points.

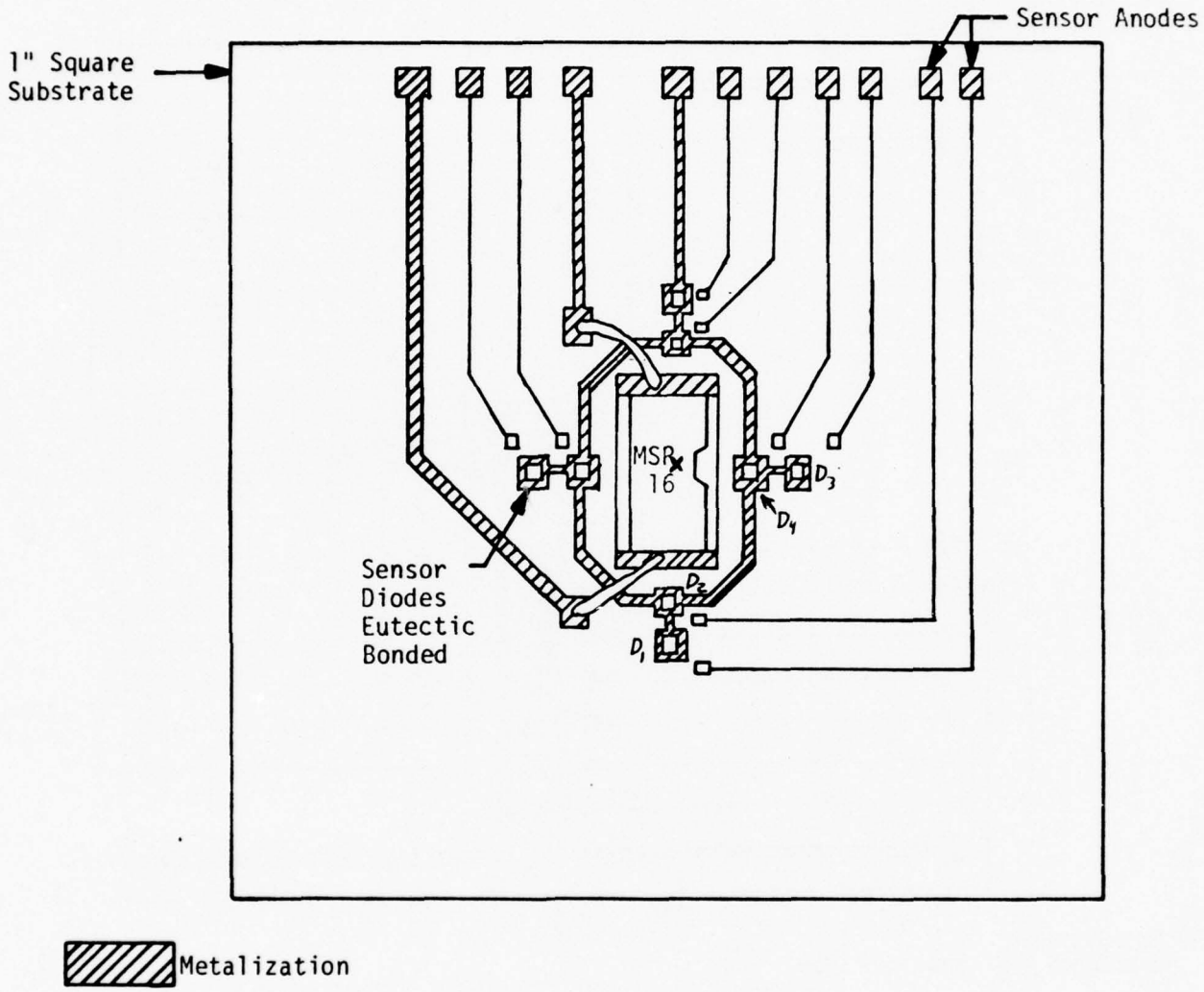

Figure 14. Chip Resistor Test Circuit Measurement Points.

IV. EXPERIMENTAL AND ANALYTICAL RESULTS

A. Temperature and Thermal Resistance Measurements

Both measured and computed results are presented here for comparison ease. Figures 10 through 14 indicate points where both measurements were made and temperatures computed. The symbol "D" with a subscript, indicates sensor diode locations. The thermal resistance is calculated by

$$\theta = \frac{T_d - T_c}{P}$$

where T_d is the device temperature in the heat generating region, T_c is the header temperature (fixed at 26°C), and P is the device power dissipation. Temperatures are in °C.

1. Untrimmed Screened Resistor. P = 3.67W. Figure 10.

	T_d	D_4	D_3	D_2	θ
Meas.	106.5°	57.3°	35.6°	31.4°	22.8°C/W
Calc.	121.4°	57°	32.5°	28.5°	26°C/W

2. Straight-Trimmed Resistor. P = 2.42W. Figure 11.

	T_d	D_4	D_3	D_2	D_1	θ
Meas.	113.3°	43.3°	30.1°	28.4°	26°	36.1°C/W
Calc.	101.7°	40.2°	29.3°	27.8°	26.8°	31.3°C/W

3. L-Trimmed Resistor. P = 2.174W. Figure 12.

	T_d	D_4	D_3	D_2	D_1	θ
Meas.	110.2°	40.6°	29.5°	28.1°	26.4°	38.7°C/W
Calc.	124.8°	38.6°	28.6°	27.4°	26.2°	45.4°C/W

4. Eutectic Bonded Transistor. P = 5.5W. Figure 13.

	T_d	D_7	D_6	D_5	D_4	D_3	D_2	D_1	θ
Meas.	83.2°	41.8°	34.4°	31.4°	30.3°	29.6°	28.5°	27.8°	10.41°C/W
Calc.	96.4°	44.4°	36.9°	32.2°	29.8°	28.5°	27.3°	26.6°	12.81°C/W

5. Conductive Epoxy Bonded Transistor. P = 5.5W. Figure 13.

	T_d	D_7	D_6	D_5	D_4	D_3	D_2	D_1	θ
Meas.	86.4°	45.4°	37.0°	31.1°	29.6°	28.8°	27.1°	26.9°	10.98°C/W
Calc.	106.3°	44.1°	36.7°	32.1°	29.7°	28.5°	27.3°	26.6°	14.6°C/W

6. Chip Resistor. P = 3.78W. Figure 14.

	T_d	D_4	D_3	D_2	D_1	θ
Meas.	73.5°	39.5°	38.1°	34.8°	31.2°	12.6°C/W

Calc. No calculated results were obtained because resistor parameters were not available.

B. Comparison of Results

Comparison of thermal resistances show deviations between measured and calculated values from 13% to 28%. Temperatures at diode sensor locations generally were in fairly close agreement. Some of the error sources are discussed below, along with comments on possible improvement of accuracy.

1. Parameter Values. Accurate material parameters, such as thermal conductivity, are not generally available from manufacturers. For example, published conductivities of Kovar can be found that vary over almost a two to one range. Wilson [16] presents an excellent disucssion of this problem. Conservative design would dictate the use of published worse case (i.e. lowest) values of conductivities available for a particular material.

2. Bonding Defects. These would tend to give a higher than actual thermal resistance. In all cases except one, the calculated thermal resistance was higher than the measured. Therefore these defects, if they existed, could not be the primary cause of difference in results.

3. Finite-Difference Model. An increase in node density will given more accurate results, if there are no other factors causing eorror. It is doubtful that this would provide a significant accuracy increase.

4. Temperature Measurement. Measurement of temperature with thermocouple probes can be accurately made by use of the differential technique. The actual probe temperature is lower, of course, than the heat generating temperature. However, by taking two sets of measurements with different power dissipation levels and adjusting the header temperature so that the

device probe temperature remains the same, the heat generating region temperature must also remain the same. The thermal resistance is then simply the ratio of the header temperature change to the device power change. The use of this thermal resistance in the equation on page 5 allows calculation of the heat generating region temperature. In all cases this temperature was higher, as expected, than the first measured probe temperature. Further, the contact resistance of the probe was changed by the application of a lacquer coating. The same thermal resistance as without the coating was obtained.

In view of the above, it is felt that the primary source of error was the uncertainty of material parameter values. The results, analytical and experimental, were sufficiently close to show the usefulness of the finite-difference modeling technique. It can be used as a tool for predicting thermal performance of a particular hybrid system. It can also be used for comparison of two or more systems employing different materials, bonding techniques, etc.

V. RECOMMENDATIONS AND SUGGESTED AREAS FOR FURTHER RESEARCH

The use of finite-difference (nodal) methods, for hybrid circuit heat flow analysis, proved to be readily adaptable, reasonably accurate, and informative. The availability of modern computer systems makes solution of systems involving even thousands of nodes feasible. The analysis of existing hybrid structures is only one area for use of this method. A preliminary evaluation of special structures and materials can be made and optimized, before fabrication.

The probe differential temperature measurement technique should be studied for degree of accuracy. This could be done by finite-difference (nodal) modeling of the hybrid system, with and without the presence of the probe. The thermocouple technique is especially valuable because of ease and the requirement for minimal instrumentation.

One important result was the drastic increase of thermal resistance for trimmed resistors. This was shown both experimentally and analytically. Hot spots will occur on the resistor surface that could drastically change the resistance value. For resistors dissipating high power, trimming should be avoided if possible, or else larger area resistors used.

The difference in thermal resistance between eutectic and epoxy bonded transistors is minimal. However, one system that deserves

further study is the use of eutectice bonding on a thick (>2mils) gold bonding pad that extends well beyond the edges of the chip. This will have a heat spreading effect that should be particularly effective on a low conductivity substrate such as alumina. A study of the heat flux density, as revealed by the node temperatures, shows it to be quite high in the area of the substrate just under the chip.

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PART 5

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TABLE OF CONTENTS

I. INTRODUCTION

Thick film resistors (TFR's) have been used for many years in hybrid microelectronic technology. An important application of this technology is the design and fabrication of linear amplifiers and analog systems which are capable of detecting very low signal levels. Since the ability of a system to detect low level signals is fundamentally limited by the noise of the system, noise performance becomes an important design criteria. In order to design low noise hybrid circuits and systems, mathematical models must be available to predict the noise performance of the individual components in the hybrid circuit.

In this work, a mathematical model is presented based on previous work and on a theoretical work to be published in the near future [10]. This model is verified by experiment for three TFR resistive pastes.

Earlier investigations have developed models to describe the noise spectral response of discrete resistors. However, the noise characteristics of TFRs have not been adequately investigated. Particularly, the effect of TFR contacts, or terminations, has not been considered separately. Previous experimental data has included both phenomena in the same measurements [8, 9]. In this work, contact noise is eliminated by the experimental method employed and thus the actual noise of the TFR itself is obtained.

II. LOW FREQUENCY NOISE MODEL

There are two types of noise found to dominate the noise spectral response of a TFR. The first type to consider is the thermal noise voltage [1], e_{th}^2, which is given by

$$e_{th}^2 = 4kTR\Delta f \qquad \text{Eq 1}$$

e_{th}^2 = mean square thermal noise voltage

where k = Boltzmann's Constant

T = Absolute Temperature

R = Resistance

Δf = Noise Bandwidth of System

Secondly, a dc current flowing through the TFR gives rise to an excess noise voltage or 1/f noise [2], which is given by

$$e_{ex}^2 = K \frac{I_{dc}^2}{f^{\alpha}} \Delta f \, R^2 \qquad \text{Eq 2}$$

where

e_{ex}^2 = Mean square excess noise

K = Constant

I_{dc} = dc current through the TFR

f = Frequency

α = Constant.

The constant K in equation 2 has been found in previous work [7, 8, 9, 10] to be dependent on the geometry and the material used in fabrication of the TFR. This relation predicts an inverse dependence on TFR volume, or

$$K = K' \frac{\rho}{\ell w t} = K' \frac{\rho_s}{\ell w} \qquad \text{Eq 3}$$

where

ℓ = Length of TFR

w = Width of TFR

t = Thickness of TFR

ρ = Bulk resistivity

ρ_s = Sheet resistivity .

The factor K' in equation 3 is a new constant which is dependent only on the firing condition and the resulting microstructural

properties of the resistor material. It is independent of the TFR geometry but it may exhibit some second order dependence on ρ_s in cases where the microstructure is altered as the resistivity is changed [7, 10].

Incorporating eq 3 into eq 2, the following expression is obtained:

$$e_{ex}^2 = K' \frac{I_{dc}^2}{f^\alpha} \frac{\rho_s^3 \ell}{\omega^3} \Delta f \qquad \text{Eq 4}$$

Since the thermal noise and the excess noise voltages are produced by independent mechanisms, the two noise components are uncorrelated. Because of this, the total noise voltage appearing at the TFR terminals may be expressed as the linear sum of the thermal component and the excess component.

$$e_{tot}^2 = e_{th}^2 + e_{ex}^2$$

$$= 4kTR\Delta f + K' \frac{I_{dc}^2}{f^\alpha} \frac{\rho_s^3 \ell}{\omega^3} \Delta f \qquad \text{Eq 5}$$

Equation 5 is the basic expression used in this work to model the TFR noise output. It gives an expression for determining the entire noise spectral output of a TFR as a function of frequency. Figure 1 shows a typical plot of the TFR noise voltage versus frequency. The break frequency, f_B, occurs when the thermal and excess noise components are equal in magnitude. Equating the two terms of

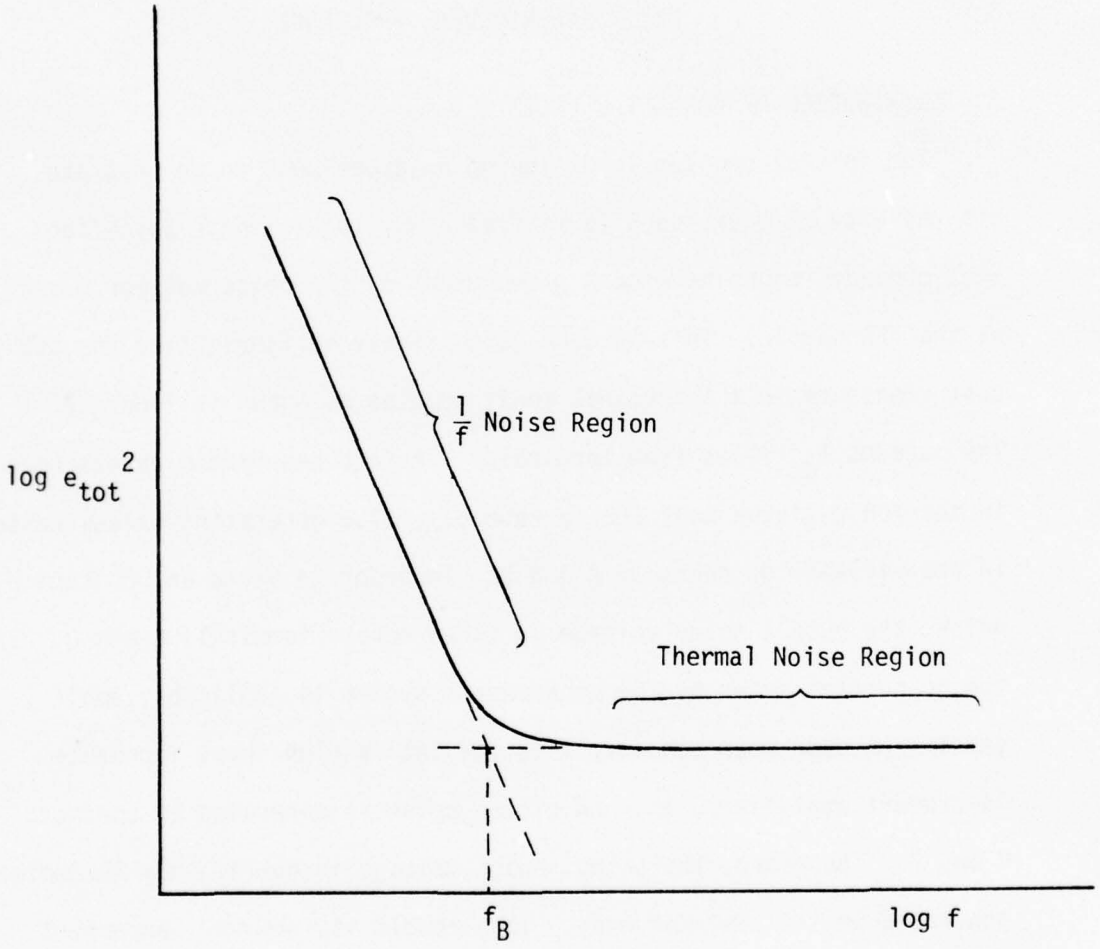


Figure 1. A typical TFR low frequency noise spectral response.

equation 5,

$$f_B = \frac{K'}{4kT} \frac{\rho_s^2 I^2}{\omega^2}$$

$$= \frac{K'}{4kT} E^2 \qquad \text{Eq 6}$$

where E = electric field across the length of the TFR.

III. EXPERIMENTAL PROCEDURE

A) ELIMINATION OF CONTACT EFFECTS

The initial problem in designing an experiment to demonstrate the validity of equation 5 is to find a way to eliminate any effect that contacts might have on a measurement of the noise voltage output of the TFR sample. This is done quite simply by fabricating the TFR test resistors in a 4-terminal configuration as shown in figure 2. The current I_{dc} flows from terminals A to B generating excess noise in the TFR resistor body and, presumably, also generating excess noise in the vicinity of contacts A and B. In order to avoid any contact noise, the output noise voltage is taken across terminals C and D. If the dc current drawn by the measurement system is negligibly small (as is the case when the output is fed into a high input impedance instrument amplifier), then no excess noise is generated at contacts C and D. Therefore, the output noise voltage is due to only the noise generated in the resistor body. This result is, however, dependent on the fact that the constant current source I_{dc} has infinite internal impedance. In figure 3 the TFR is modeled as a network of

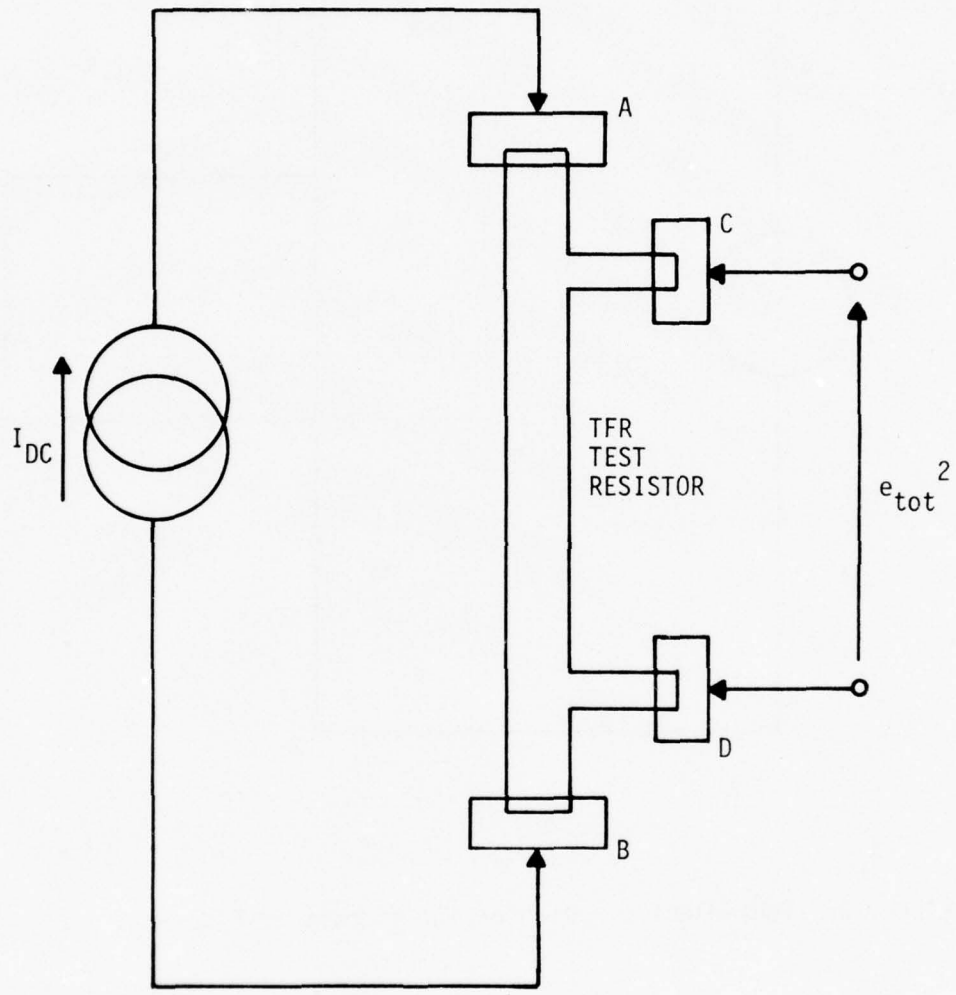


Figure 2. Circuit configuration used to exclude contact noise from measurement.

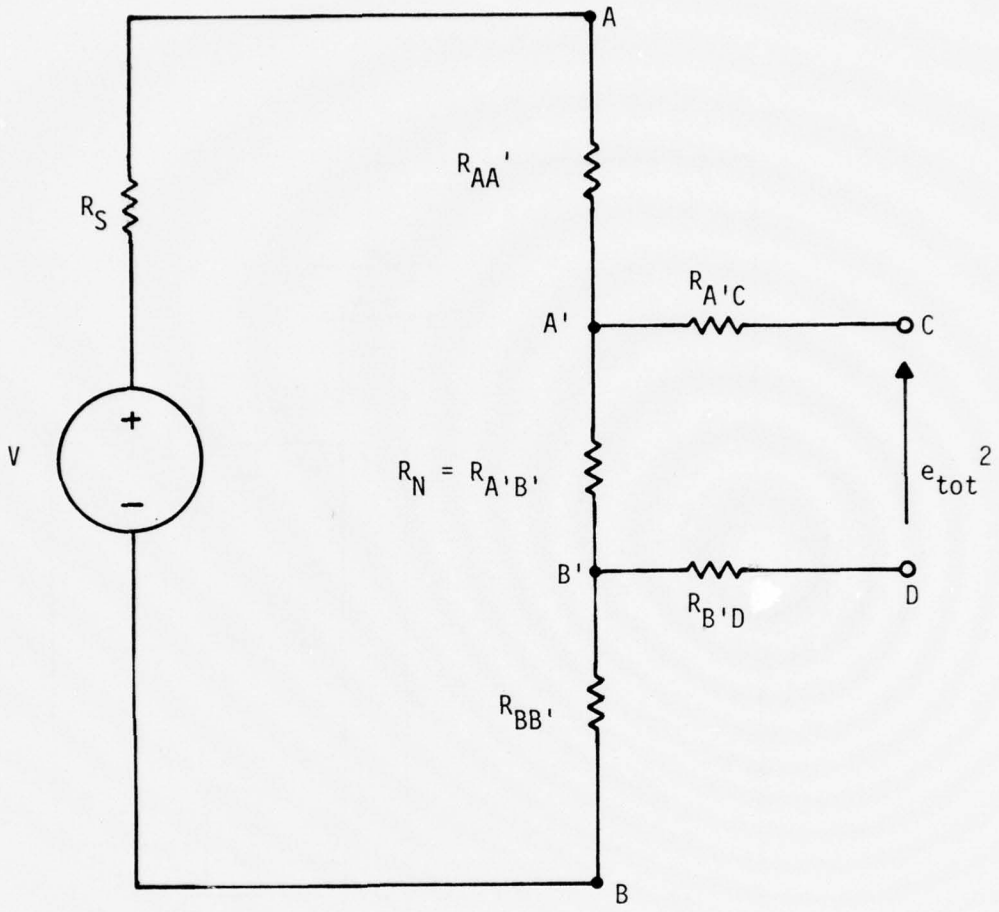
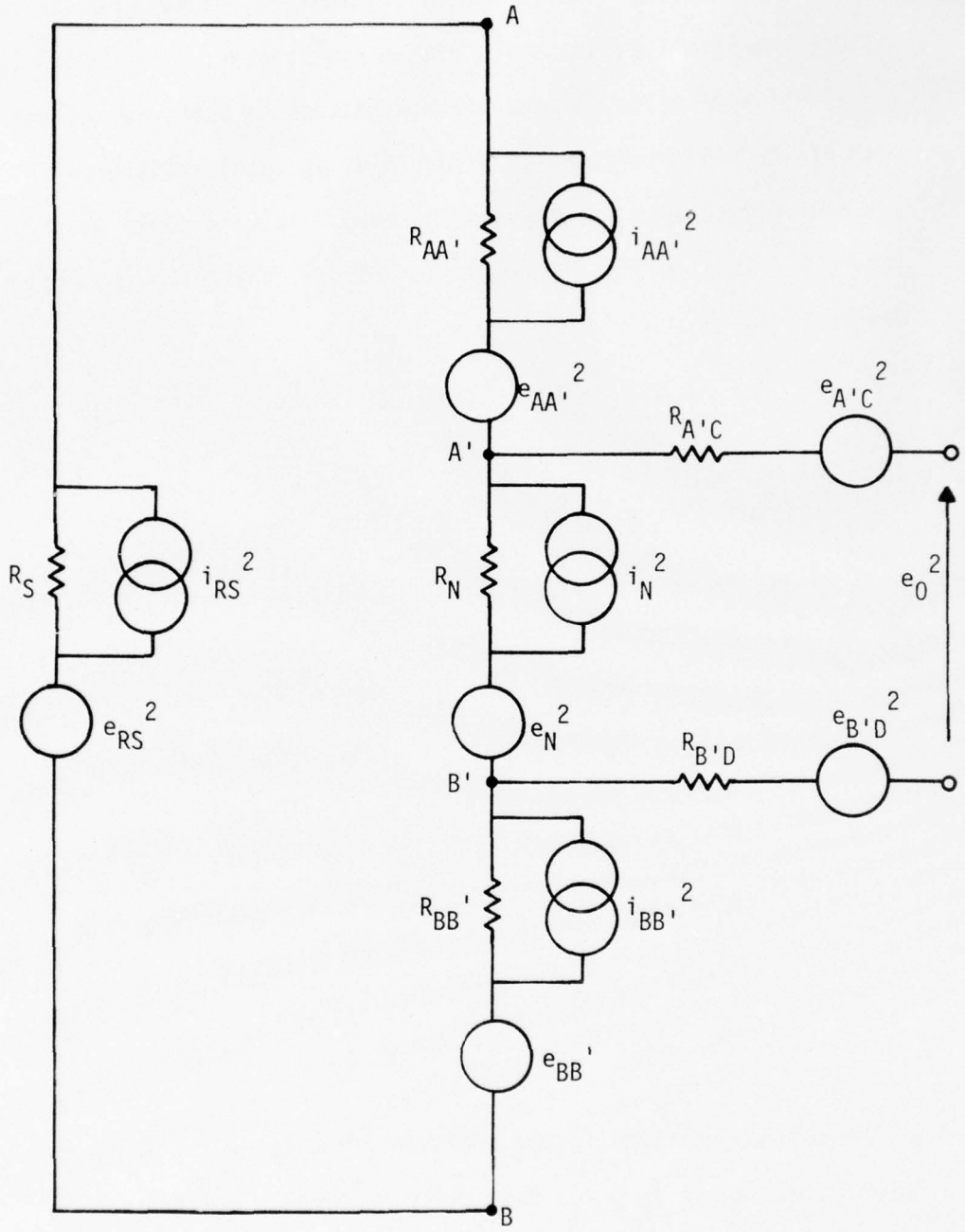


Figure 3. Equivalent circuit for the circuit in Figure 2.



e_{xx}^2 = mean square thermal noise voltage of R_{xx}

i_{xx}^2 = mean square excess noise current of R_{xx}

Figure 4. Noise equivalent circuit for the circuit of Figure 2.

resistors and the current source is modeled realistically as an ideal voltage generator, V, in series with a resistor Rs.

The output noise voltage of this network is found by replacing each of the real resistors in figure 3 by an ideal resistor with the appropriate noise generators inserted. This is shown in figure 4. To simplify the expression for e_o^2, the following assumptions may be made;

$$R_{AA'} = R_{BB'} \triangleq R_A \qquad i^2_{AA'} = i^2_{BB'} \triangleq i^2_A \qquad e^2_{AA'} = e^2_{BB'} \triangleq e^2_A$$

$$R_{A'C} = R_{B'D} \triangleq R_B \qquad e^2_{A'C} = e^2_{B'D} \triangleq e^2_B$$

The resulting expression for the mean square output noise voltage, e_o^2, is given by

$$e_o^2 = \frac{(e^2_{RS} + 2e^2_A)R^2_N}{(R_N + 2R_A + R_S)^2} + \frac{i^2_{RS}\, R^2_N\, R^2_S}{(R_N + 2R_A + R_S)^2}$$

$$+ \frac{i^2_A\,(2R^2_A)\,R^2_N}{(R_N + 2R_A + R_S)^2} + [e^2_N + R^2_N i^2_N]\,\frac{(2R_A + R_S)^2}{(R_N + 2R_A + R_S)^2}$$

$$+ 2e^2_B \qquad \text{Eq 7}$$

If the constant current source resistance R_S, is chosen to be suitably large, i.e., $R_S >> R_N + R_C$, then the output noise voltage may be approximated as

$$e_o^2 \simeq i_{RS}{}^2\, R_N^2 + 2e^2_B + e^2_N + i^2_N R^2_N \qquad \text{Eq 8}$$

It can be seen in equation 8 that two undesirable terms appear in the output. One term is due to the excess noise of the series resistor, R_S, and the other is due to the thermal noise of the resistors $R_{A'C}$ and $R_{B'D}$ in figure 4. When this technique for eliminating contact effects is actually implemented, steps must be taken to assure that the two undesirable terms are either negligible, or cancelled by the measurement technique.

In order to determine the effective value of resistance for that portion of the TFR body in which the output noise voltage is generated, R_N, the following equation is used (refer to figure 3).

$$R_N = \sqrt{R_{AB}(R_{CD}-R_{CDS})} \qquad \text{Eq 9}$$

where $R_N = R_{A'B'}$ (Figure 3)

R_{AB} = Resistance seen between terminals A and B

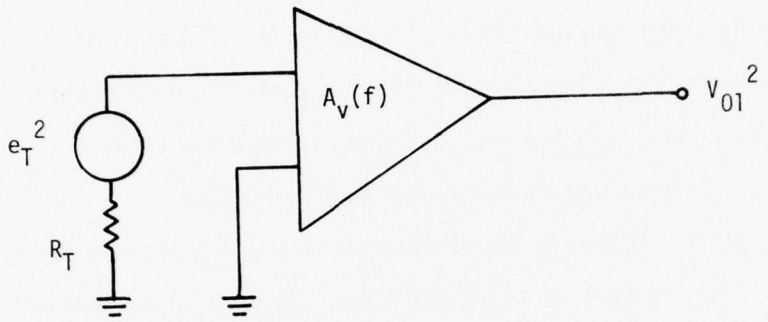
R_{CD} = Resistance seen between terminals C and D

R_{CDS} = Resistance seen between terminals C and D with terminals A and B shorted.

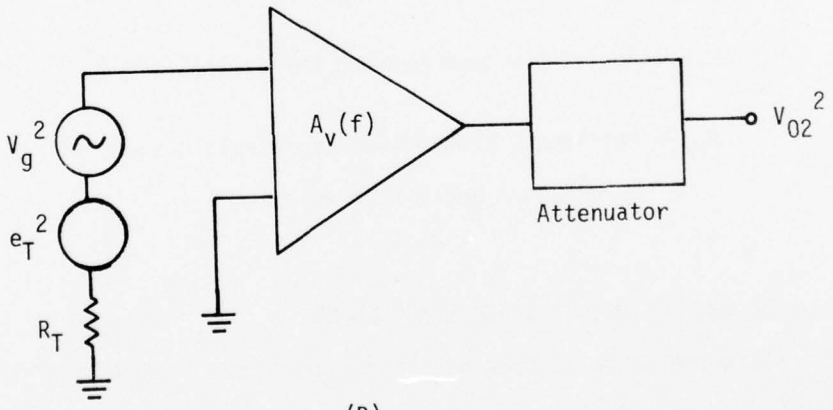
B) SINE WAVE METHOD OF NOISE MEASUREMENT

Since the noise voltage developed across the terminals of the TFR cannot be measured directly, an indirect method known as the sine wave method [3] is employed.

Consider the circuit shown in figure 5A. If e_T^2 is the mean square noise voltage of a test resistor, R_T, then the amplifier mean



(A)



(B)

Figure 5. Sine wave method of noise measurement.

square output voltage, v_o^2, is given by

$$v_{o_1}^2 = A_V^2 (f)\ e_T^2 \qquad \text{Eq 10}$$

where $A_V(f)$ is the voltage gain of the amplifier.

If a known attenuation is now inserted into the gain path and a sine signal is inserted serially with the test resistor, as in figure 5B, as new equation may be written;

$$V_{o_2}^2 = A_V^2 (f)\ (e_T^2 + V_g^2\ )\ (\text{atten})^2 \qquad \text{Eq 11}$$

If the special case where $V_{o_1} = V_{o_2}$ (by adjustment of either the magnitude of V_g or (atten)) is assumed, then the mean square noise signal at the input is

$$e_T^2 = V_g^2\ \frac{(\text{atten})^2}{1 - \text{atten}^2} \qquad \text{Eq 12}$$

This equation may be used in the determination of the input noise voltage when the stated conditions are met.

C) IMPLEMENTATION OF THE MEASUREMENT SYSTEM

The actual circuit used in the measurement system is given in figure 6. The system includes five major components which are listed and discussed below.

1. Constant Current Source

The circuit for the constant current source is the result of considerable trial and error experimentation. The value of the

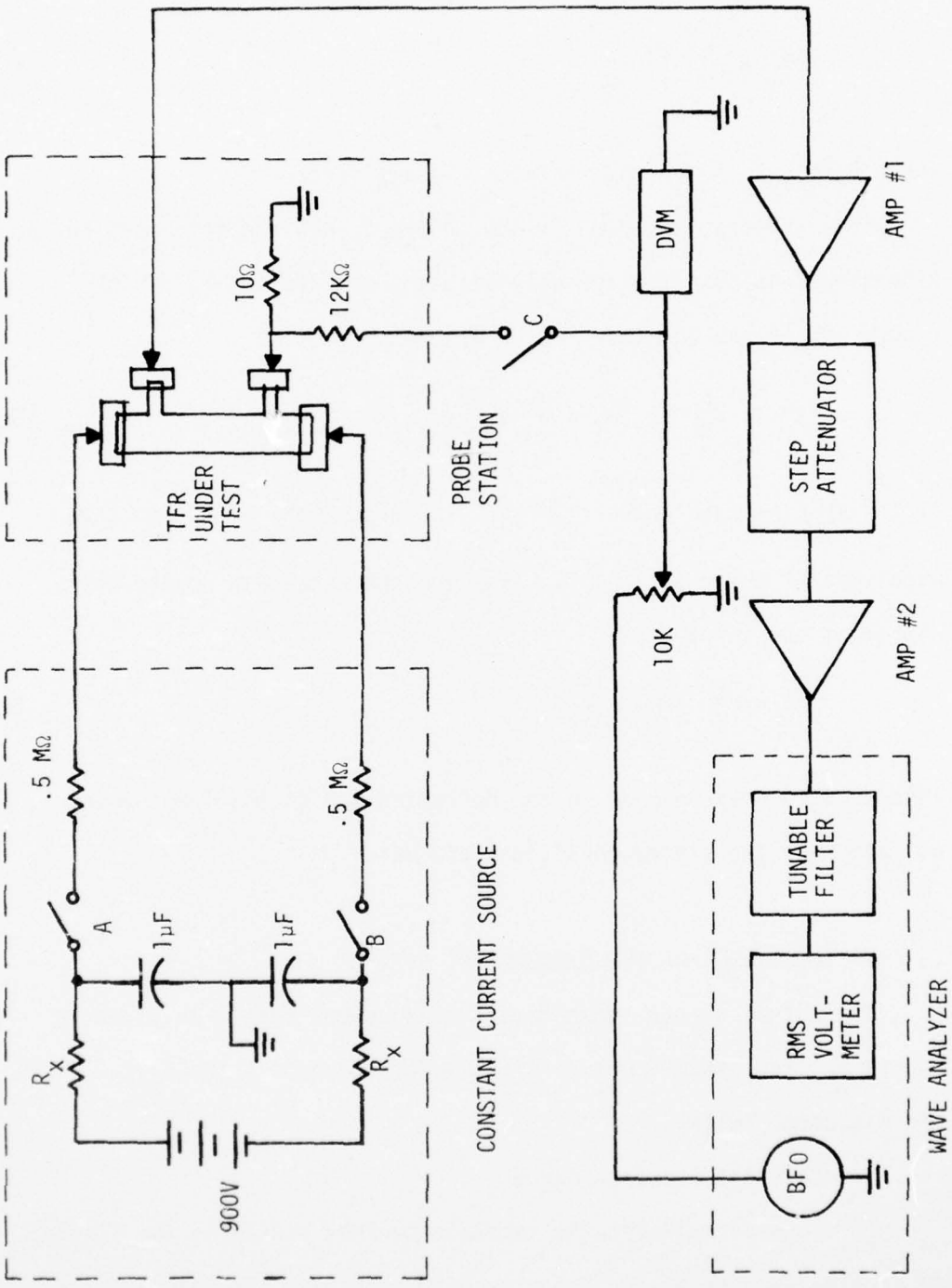


Figure 6. Actual Measurement System

resistors Rx are changed to obtain a given constant current output value. Any noise generated by Rx or the 900v battery is shunted to ground by the 1 microfarad capacitors. In addition, the .5 Megohm resistors are wirewound to preclude the generation of excess noise. This point is of paramount consideration in the source design because, as can be seen in equation 8, any noise generated by the current source will appear in the noise measurement.

2. Probe Station

The probe station consists of a copper-clad box with a hinged lid for easy access. The base is of a 1 1/2 inch thickness of steel plate with a 3/4" well in the middle. The TFR sample under test is positioned in the well and electrical contact to the TFR is made through four magnetic-base probes positioned around the periphery of the well (See figure 7).

3. Instrument Amplifiers

In figure 6, there are two amplifiers inserted in the signal gain path. From equation 12 it can be seen that the actual gain of the amplifiers is not a factor in determining the noise level input to the system. However, the signal must be of sufficient magnitude to drive the wave analyzer input. The actual circuitry for the two amplifiers is shown in figure 8, along with performance characteristics. A 12 volt lead-acid battery is utilized as a low noise supply. Amplifier A is of low noise design while the noise performance of Amplifier B is negligible, because of the relatively high signal level at its input. As will be pointed out later, the noise of the system is eliminated by experimental procedure.

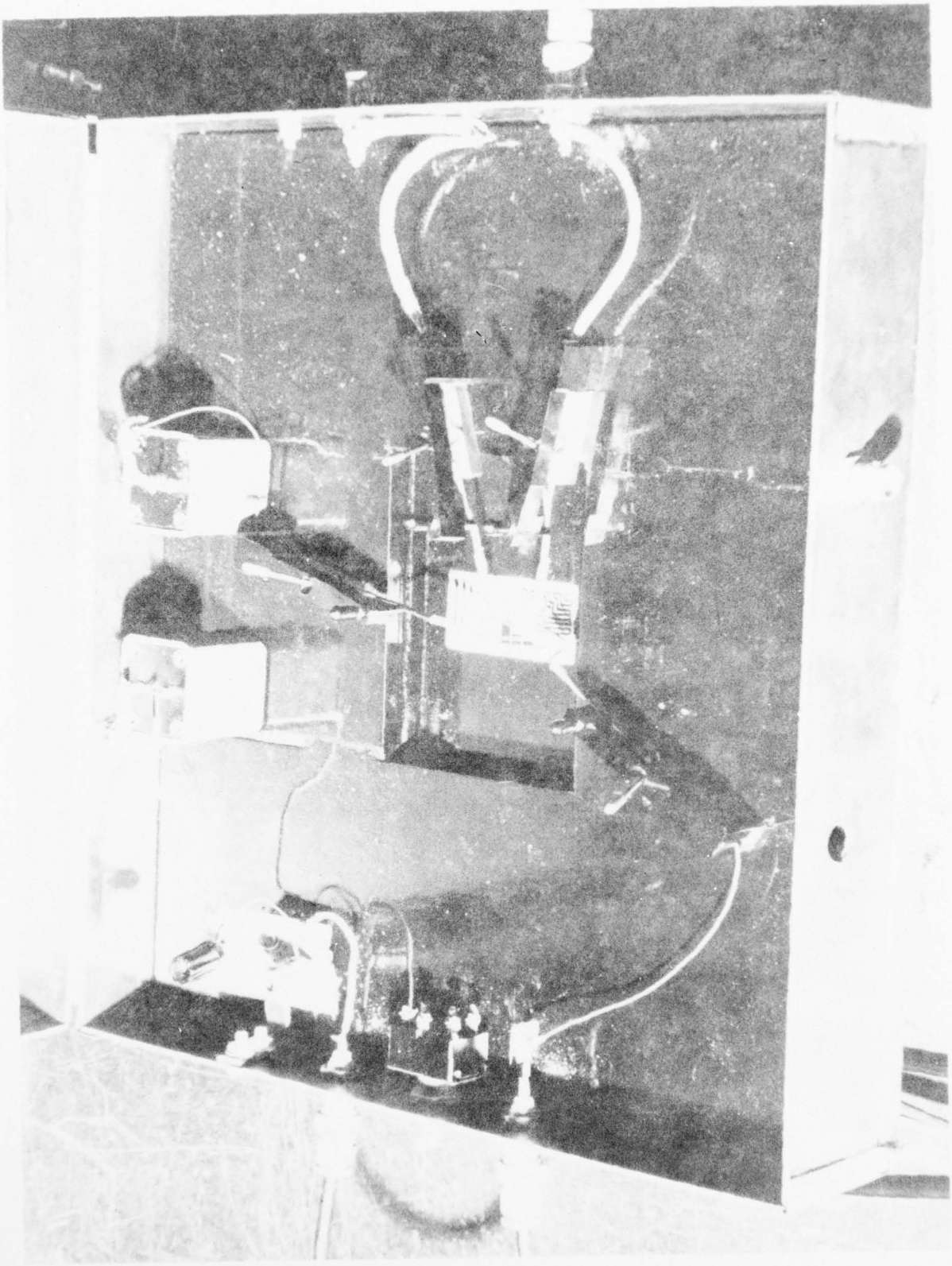


Figure 7. Photograph of the probe station

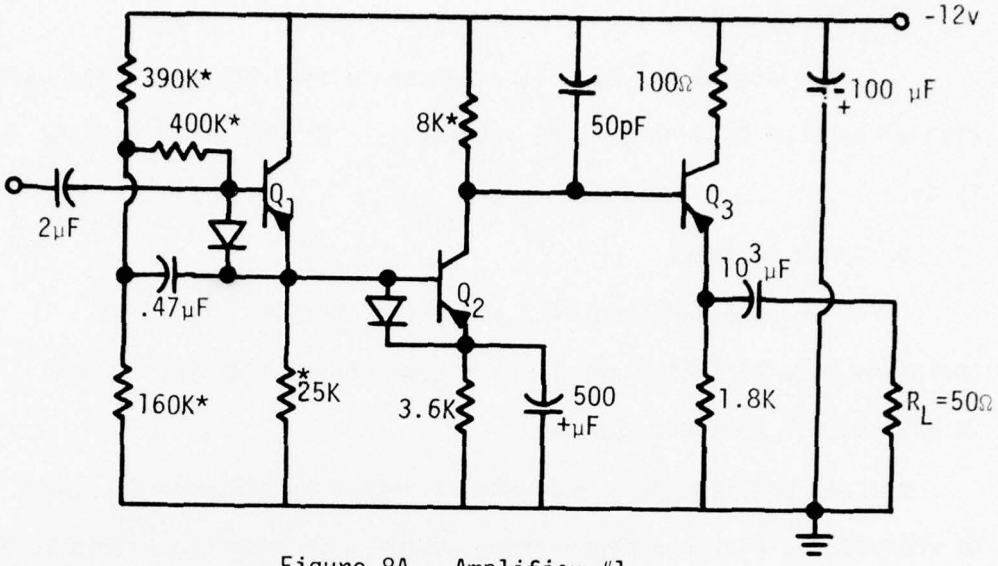


Figure 8A. Amplifier #1

A_v = 100 f_{Hi} = 300 KHz NF = 1.3 dB

R_i = 2MΩ f_{LO} = 5 Hz @ 20 Hz, R_N = 30 KΩ

Q_1, Q_2, Q_3 are Sylvania ECG 234, Low Noise, Beta = 400.
* low noise

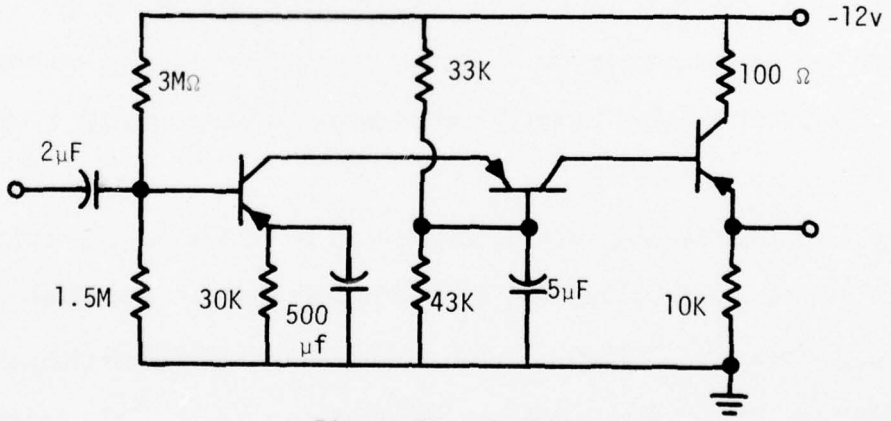


Figure 8B. Amplifier #2

A_v = 75 f_{HI} = 400 KHz

R_i = 75 KΩ f_{LO} = 3 Hz

4. Attenuator

The attenuator used is a Tektronix 2701 50Ω step attenuator, with a range of 0-79 dB in 1 dB increments. Its passband extends down to dc.

5. Wave Analyzer

The wave analyzer is a Quan Tech 304 TDL. The 3-Hz (noise bandwidth) filter and a meter time constant of 100 seconds is used on all measurements.

Several problems were encountered during the course of attempting to implement a workable measurement system. In order to eliminate E-M interference, the bias source, probe station, and amplifiers were each constructed in copper-clad enclosures and all interconnections were made with 50Ω shielded cable. After experiencing persistent problems with interference, the system was moved to a screen room.

Because of the shielding employed, ground loops were found to be coupling in excessively large 60Hz signals. This was solved by breaking the ground connection in one of the interconnecting cables. The most effective point to apply this remedy is found through trial and error.

Another interference problem was traced to mechanical vibration. Because of the low frequency region of interest and the low-level signals involved, vibration originating with, for example, air-conditioning equipment in the building causes an interfering signal. This problem was solved by resting the entire table (on which the system rested) on four $1ft^2$ plywood plates, underneath each of which is a 6 inch deep by $1ft^2$ foam cushion. Additionally, the most sensitive components of the system

(bias supply, probe station, and amplifiers) rested on foam cushions several inches thick. This arrangement effectively dampens the mechanical vibrations.

Due to the fact that a common supply is used for both amplifiers, the possibility exists for strong signal coupling around the attenuator. This problem is avoided by employing a supply bypass capacitor at each amplifier.

D) OPERATIONAL PROCEDURE

To measure the excess noise of a particular TFR, it is first positioned in the probe station with the probes contacting the appropriate terminal. Then resistors Rx are adjusted to give a desired current. After tuning the wave analyzer to a desired frequency the following steps are performed:

1. Open switches A, B, and C and set attenuator to 0dB. Record the output level of the Quan Tech meter. Several meter time constants (100 sec.) must be allowed for the meter to reach steady state.

2. Set the attenuator to some value, say 60 dB, and close switch C. The potentiometer is adjusted until the Quan Tech meter reads the same level as in step 1. The noise input is then calculated according to equation 12 where v_g = (voltage indicated by DVM)X $\frac{10\Omega}{12K\Omega}$. Note that if the attenuation is sufficiently high then equation 12 becomes

$$e_T^2 \simeq v_g^2 \,(\text{atten})^2 \,.$$

Because the output meter on the wave analyzer is an average reading meter, the value obtained is not the true rms value for a noise signal. However, correction may be made for this fact by adding 1dB [6] to the existing attuation level.

The noise voltage calculated at this point is the sum of the thermal noise of the TFR and system noise.

3. Repeat steps 1 and 2 except switches A and B are left closed to provide dc current to the TFR. The noise voltage calculated here is the sum of the excess and thermal noise of the TFR, and system noise.

4. The excess noise generated by the TFR is the difference in the two calculated voltages, or

$$e_{ex}^2 = \left[\begin{matrix}\text{noise voltage} \\ \text{from part 3}\end{matrix}\right] - \left[\begin{matrix}\text{noise voltage} \\ \text{from part 2}\end{matrix}\right] \qquad \text{Eq 13}$$

Note that the excess voltage calculated is for a Δf centered at some frequency. The spot noise in volts^2/Hz is found by dividing the above equation by Δf.

The measurement procedure described cancells both system noise and the thermal terms present in equation 8. However, it must be further demonstrated that the term $i_{RS}R_N$ (equation 8) is negligible. In other words, for accurate measurement, the noise contribution of the constant current source must be negligible. In order to experimentally assure this condition, a wire-wound resistor of known value ($\tilde{}$ 20K) is probed. For $I_{DC} = 0$, the resulting measurement is due to the sum of the system noise and the resistor's thermal noise which can be calculated (equation 1). Since the 1/f noise of a

quality wire-wound resistor is negligible, no increase in noise should be detected when $I_{dc} \neq 0$.

The noise band width of the filter in the Quan Tech Wave analyzer is determined by a graphical integration according to the equation [5],

$$\Delta f = \frac{1}{G_o} \int_o^\infty G(f)\, df. \qquad \text{Eq 14}$$

where $G(f)$ = power gain as function of frequency

G_o = peak power gain.

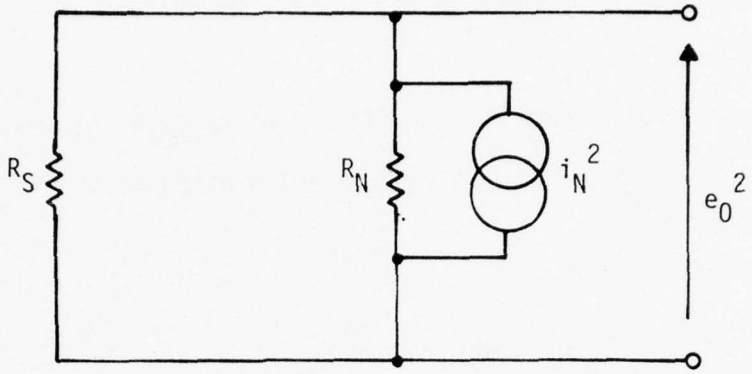
The procedure is to obtain a curve of the output voltage of the filter as a function of frequency, for a constant input voltage. Then, this curve is graphically squared. The area under the resulting curve divided by the peak of the curve is the noise bandwidth, Δf.

E) LIMITATIONS OF MEASUREMENT SYSTEM

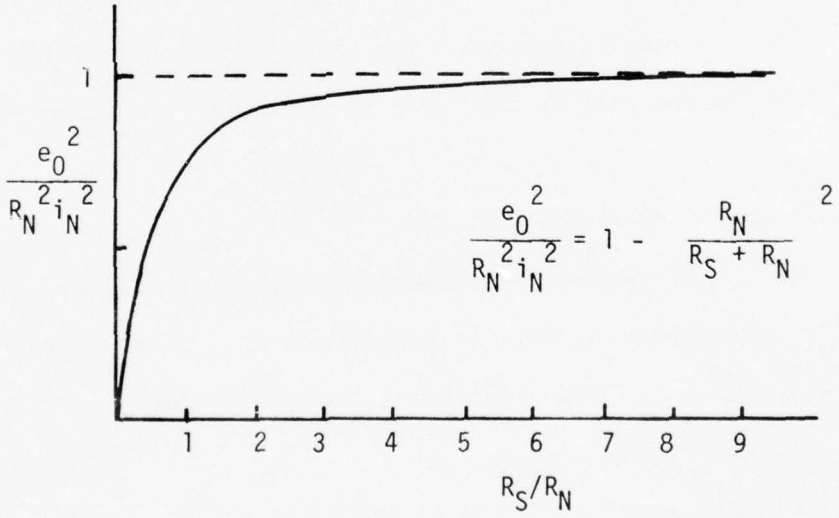
Because of the simplifying assumptions made in the development of the measurement system, certain limitations must be imposed on the operation of the system. These are discussed below.

1. Allowable values for R_N

The maximum allowable value for R_N is a function of the impedance of the current source, R_S. Figure 9A shows an AC equivalent circuit for the constant current cource and the body of the TFR. The thermal noise sources are not considered here, as they are cancelled from the measurement, anyway.



(A)



(B)

Figure 9. The effect of R_S on the output noise of the TFR.

From figure 9A, then, the noise output, e_o^2, is

$$e_o^2 = R_N^2 \; i_N^2 \left[1 - \left(\frac{R_n}{R_S+R_N}\right)^2\right] \qquad \text{Eq 15}$$

A normalized plot of e_o^2 vs R_S is shown in figure 9B. The curve approaches a plateau when $R_S \geq 8\ R_N$. For R_S = 1mΩ, then, R_N must be limited to less than approximately 125kΩ. However, if the input impedance of the instrument amplifier is considered in shunt with R_S, then R_N must be limited to less than approximately 80kΩ (for an input impedance of 2mΩ).

2. Low Level Limit of Excess Noise Measurement.

The lowest level of 1/f noise that can be measured by the system is limited by the thermal noise of R_N, and by system noise. Since a determination of the excess noise level involves taking the difference between two separate measurements, if the value of e_{ex}^2 is much smaller than the system noise and the thermal noise of R_N then it has the same order of magnitude as the experimental error. Typically, consistent data is obtained at a minimum e_{ex}^2 of approximately the same level as the sum of system and thermal noise of R_N.

3. Accuracy

The theoretical limit of accuracy of the measurement system must be determined from a statistical approach, due to the random nature of a noise voltage. A relation [4] between noise bandwidth, Δf, output meter time constant, τ, and relative error, σ, is

$$\sigma = \frac{1}{\sqrt{2\tau\Delta f}}. \qquad \text{Eq 16}$$

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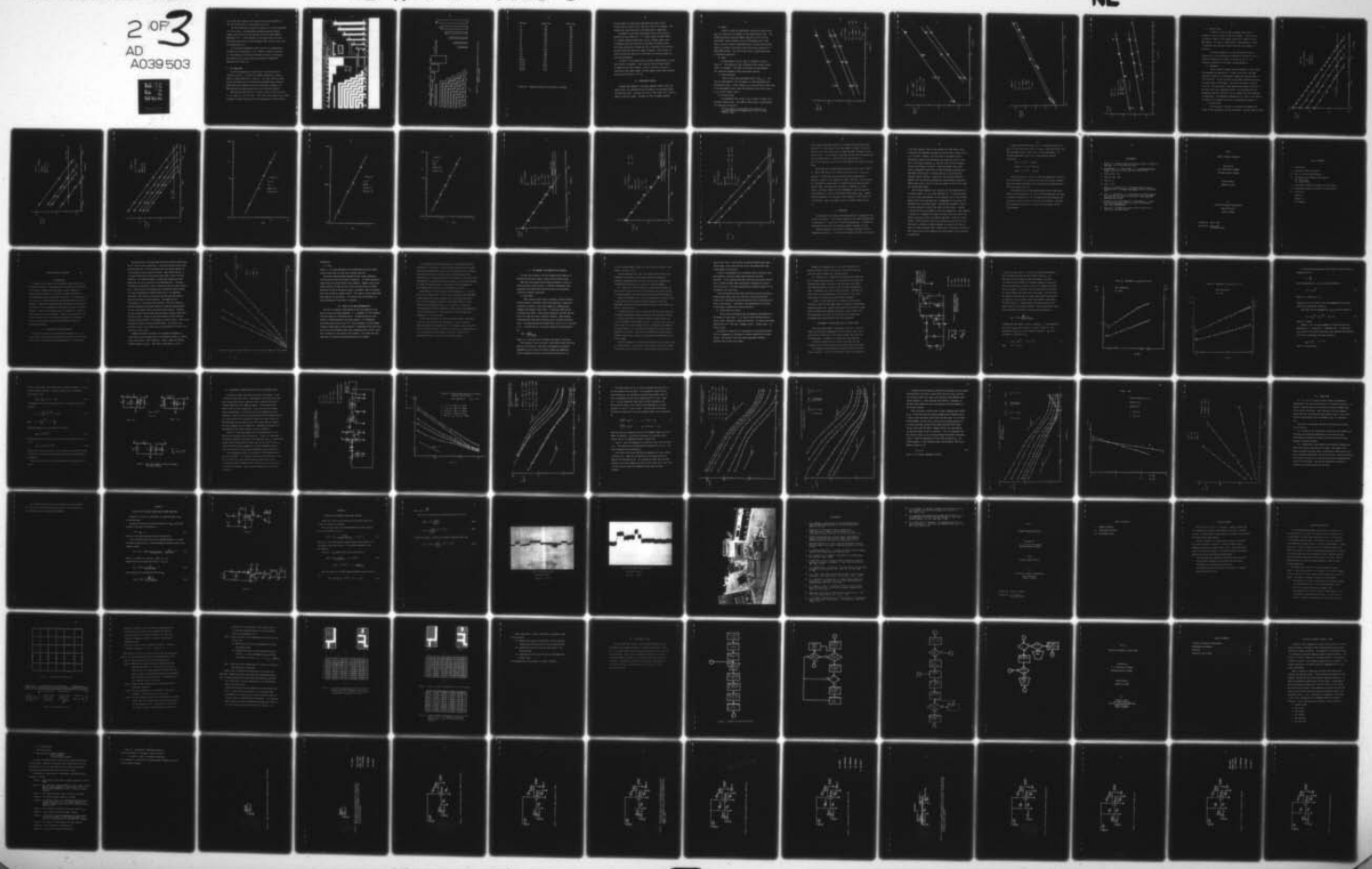


For a meter time constant of 100 seconds and a noise bandwidth of 3Hz, the relative error is approximately .04 or 4%.

The error predicted by equation 16 applies to a single measurement of a noise signal. The measurement technique employed, however, computes excess noise as the difference of two such measurements. Depending on the relative magnitude of the excess noise, the error (for excess noise) may vary from acceptably small values to very large and unacceptable error.

For the actual measurement system, the error is conservatively estimated to be approximately $\pm$ 10%. However, scatter in the data is also effected by variation of parameters external to the measurement system, such as noise pickup and variation of geometrical dimensions of the TFR, etc.

F) TFR FABRICATION

The TFR test samples were fabricated in the microelectronic laboratory of the U. S. Army Missile Command, Huntsville, Alabama. A sample is shown pictorially in figure 10. The three resistive pastes used are ESL 3000 series (iridium based) with 8835-1B gold conductor, DuPont 1400 series (ruthenium based) with 8760 gold conductor, and EMCA 5000 series (ruthenium base) with Firon 212B gold conductor.

Each type ink was mixed for six nominal values of sheet resistance; 1Ω, 10Ω, 100Ω, 1kΩ, 10kΩ and 100kΩ. These pastes were checked with a Haake viscometer to ensure compliance with the manufacturer's specifications.

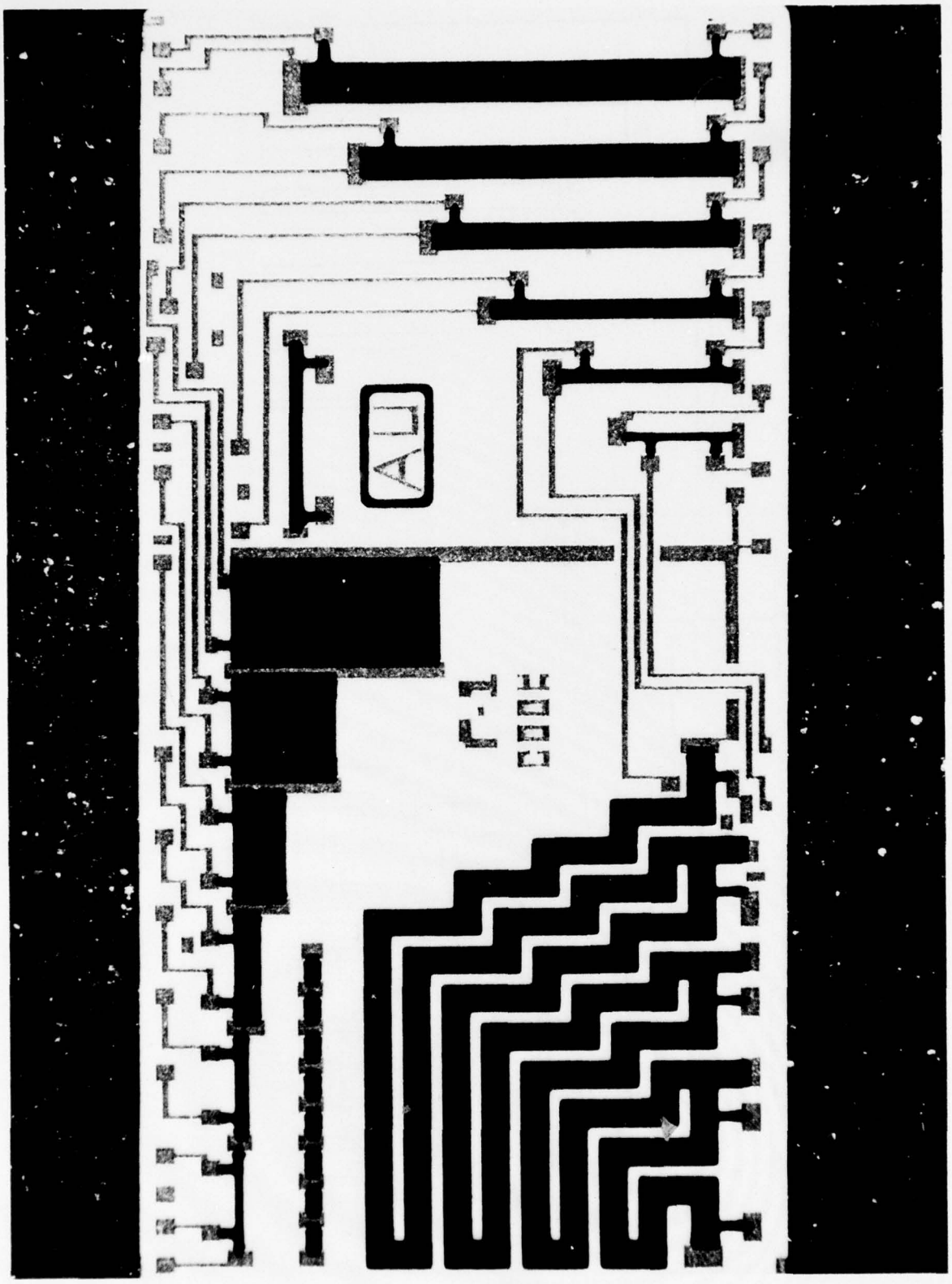


Figure 10. Photograph of a TFR test sample.

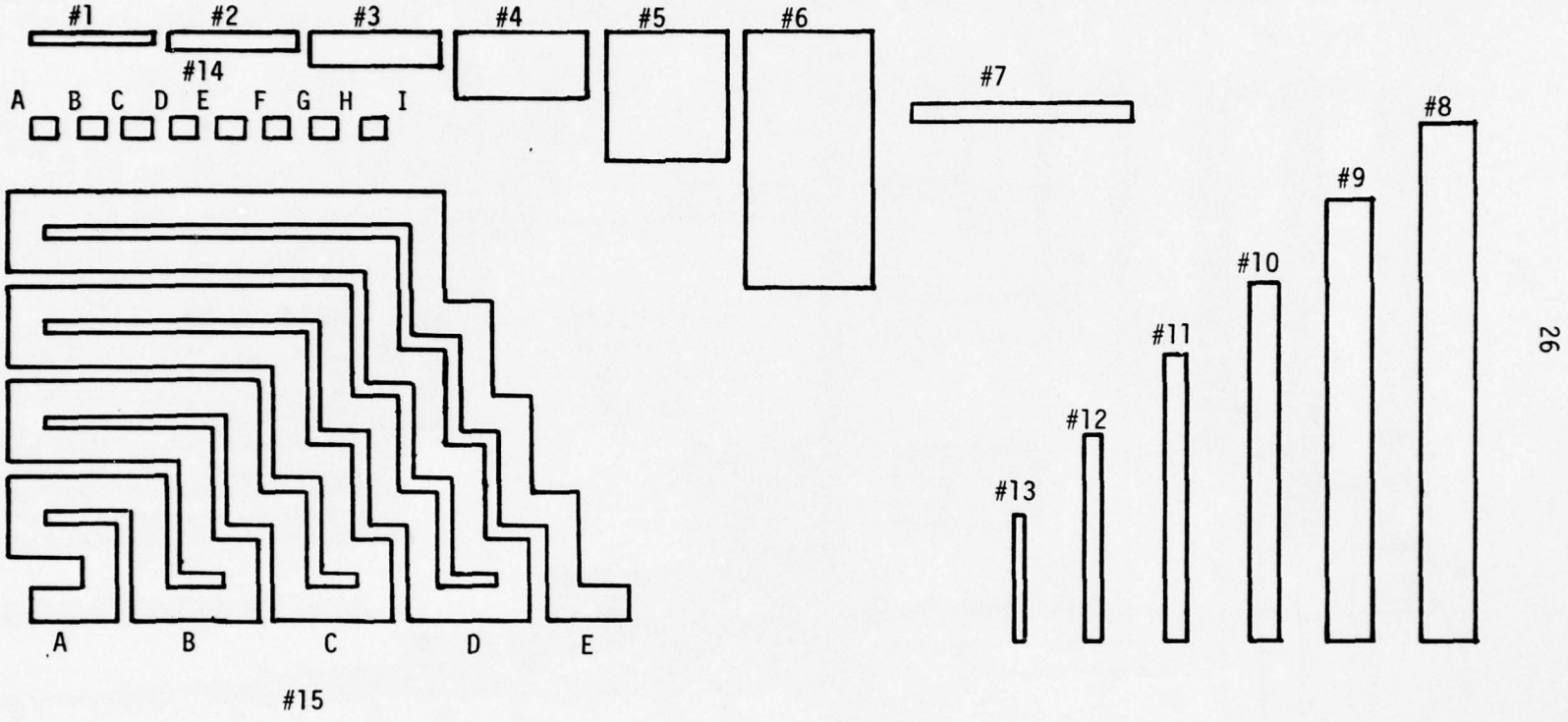


Figure 11A. System of resistor identification on a particular substrate (sample).

Resistor	Length (cm)	Width (cm)
#1	.254	.025
#2	.254	.051
#3	.254	102
#4	.254	.203
#5	.254	.406
#6	.254	.813
#7	.610	.051
#8	1.52	.152
#9	1.27	.127
#10	1.02	.102
#11	.762	.076
#12	.508	.051
#13	.254	.025
#14 AI	.762	.051
#15 AE	13.7	.102
#15 BE	8.38	.102
#15 CE	4.27	.102
#15 DE	1.44	.102

Figure 11B. Dimensions of R_N for the resistors indicated.

Various numbers of samples were fabricated from each of the 6 resistivities for each of the 3 inks for a total of 114 samples. The samples were fired according to the manufacturer's suggestions.

The geometric variations incorporated into the test resistor patterns are (see figure 10): 1) constant width, variable length, 2) constant length variable width, and 3) constant aspect ratio. In addition, two extra resistors are provided, one normal and one with extra terminations included serially in the body of the resistor, but both having the same total number of squares. This was done in order to allow some insight as to the effect of resistor contacts on the noise performance.

In figure 11, the system used for resistor identification is given. Each resistor is numbered. Also, resistors 14 and 15 have letters to identify their extra contacts. Thus, a particular resistor is identified by the sample number, resistor number, and by which contacts were used (for resistor 14 or 15).

IV. EXPERIMENTAL RESULTS

Although three geometric variations (constant length, width, and aspect ratio) are available on the TFR samples, only constant length and width were used. The reason for this is that aspect ratio does not appear in the noise model. Thickness of TFRs is assumed constant.

A) Length

Figure 12 gives the experimental variation of excess noise, e_{ex}^2, as a function of TFR length, for the three different inks. The lengths available on the TFR samples range from 1.5cm to 13.7cm. The nominal* sheet resistance, (ρ_S), of the samples used is 100Ω. Lower ρ_S did not produce a measureable level of excess noise and the higher ρ_S resulted in too large a value for R_N (see Limitations of Measurement System). The slope of the curves is approximately one as prediced by equation 5.

B) Width

An experimental curve for e_{ex}^2 vs $(1/\text{width})^3$ is given in figure 13. From equation 5, e_{ex}^2 is expected to be inversely proportional to $(1/\text{width})^3$. The slope of the curves are approximately one, indicating agreement within experimental accuracy.

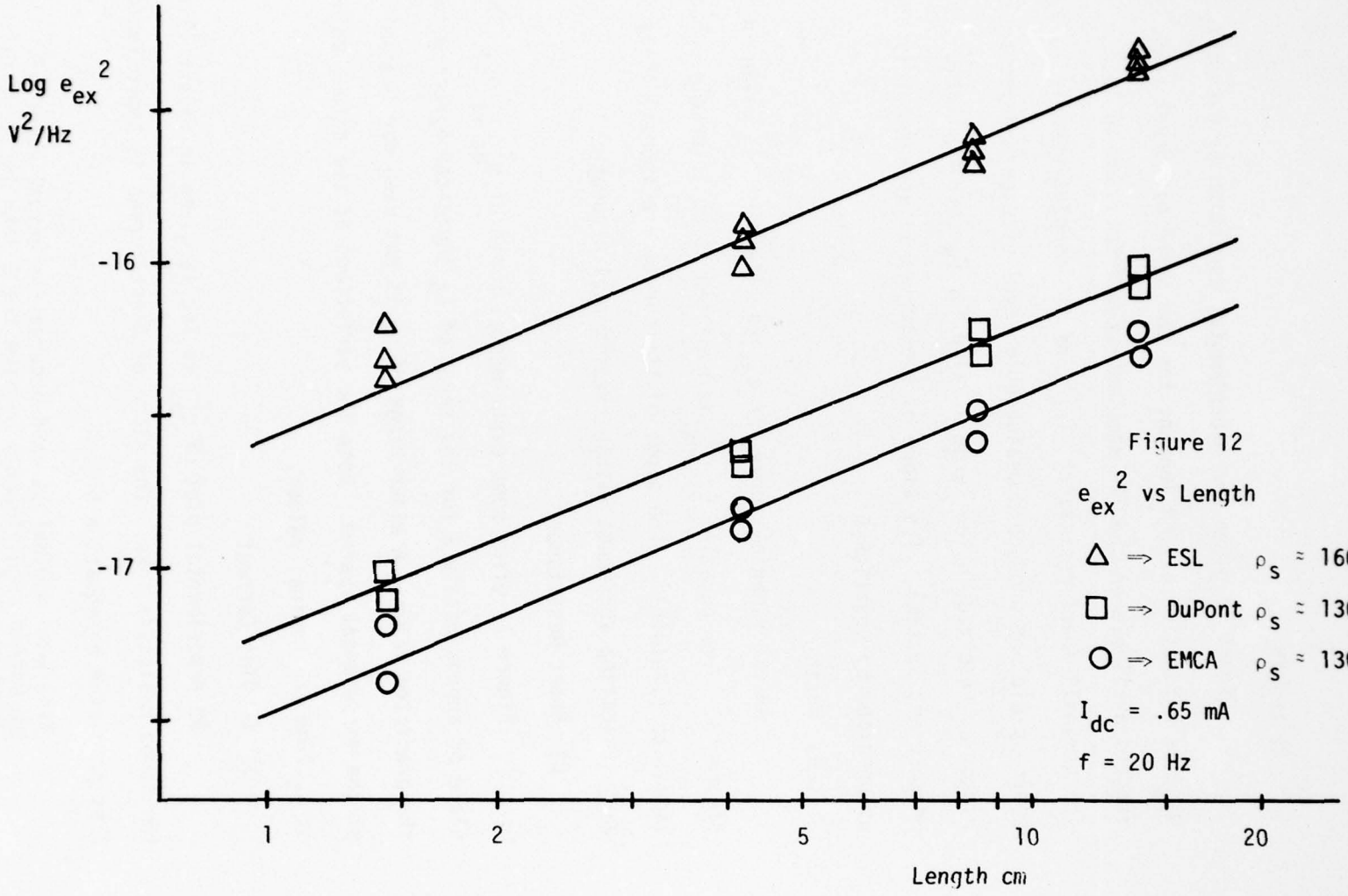
C) Sheet Resistance

Figure 14 gives some experimental plots of e_{ex}^2 vs ρ_S. The slope of approximately 3 for the range of ρ_S indicated agrees with the predicted value. A wider range of ρ_S is not used due to limitations of the measurement system. Note the variations of the actual values of ρ_S from the nominal values.

D) DC Bias Current

An experimental plot of e_{ex}^2 vs Idc is given in figure 15 for the three resistive inks. The slope of these curves is approximately 2 as predicted by equation 5.

*The word nominal is used because the actual value of ρ_S varied significantly between the 3 inks for a given "nominal" value.


Log e_{ex}^2
V^2/Hz
-16
-17
1
2
5
10
20
Length cm
Figure 12
e_{ex}^2 vs Length
△ ⇒ ESL $\rho_s \approx 160\Omega$
□ ⇒ DuPont $\rho_s \approx 130\Omega$
○ ⇒ EMCA $\rho_s \approx 130\Omega$
I_{dc} = .65 mA
f = 20 Hz

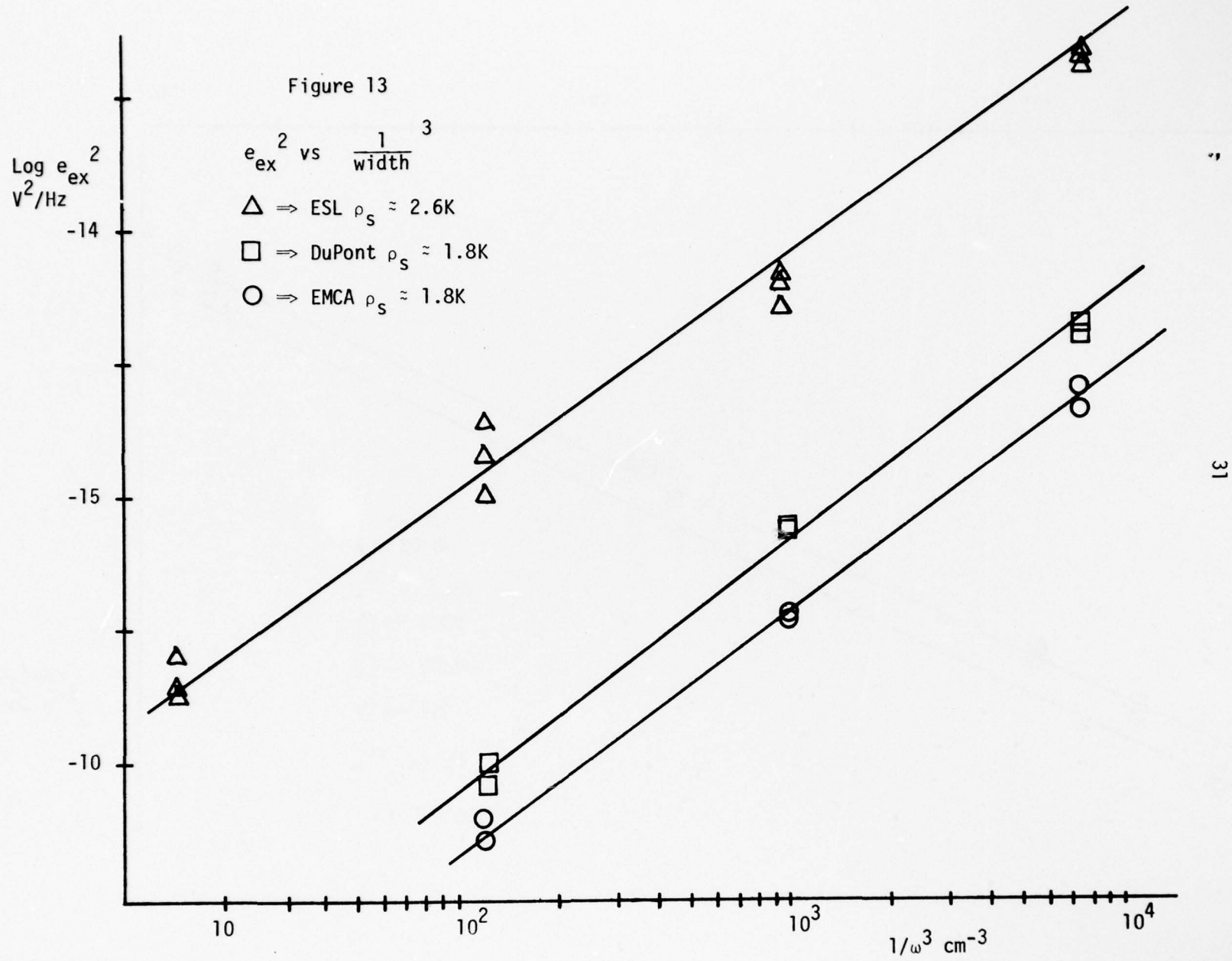


Figure 13
e_{ex}^2 vs $\left(\frac{1}{\text{width}}\right)^3$
△ ⇒ ESL $\rho_s \simeq 2.6K$
□ ⇒ DuPont $\rho_s \simeq 1.8K$
○ ⇒ EMCA $\rho_s \simeq 1.8K$
Log e_{ex}^2 V^2/Hz
-14
-15
-10
10
10^2
10^3
10^4
$1/\omega^3$ cm^{-3}

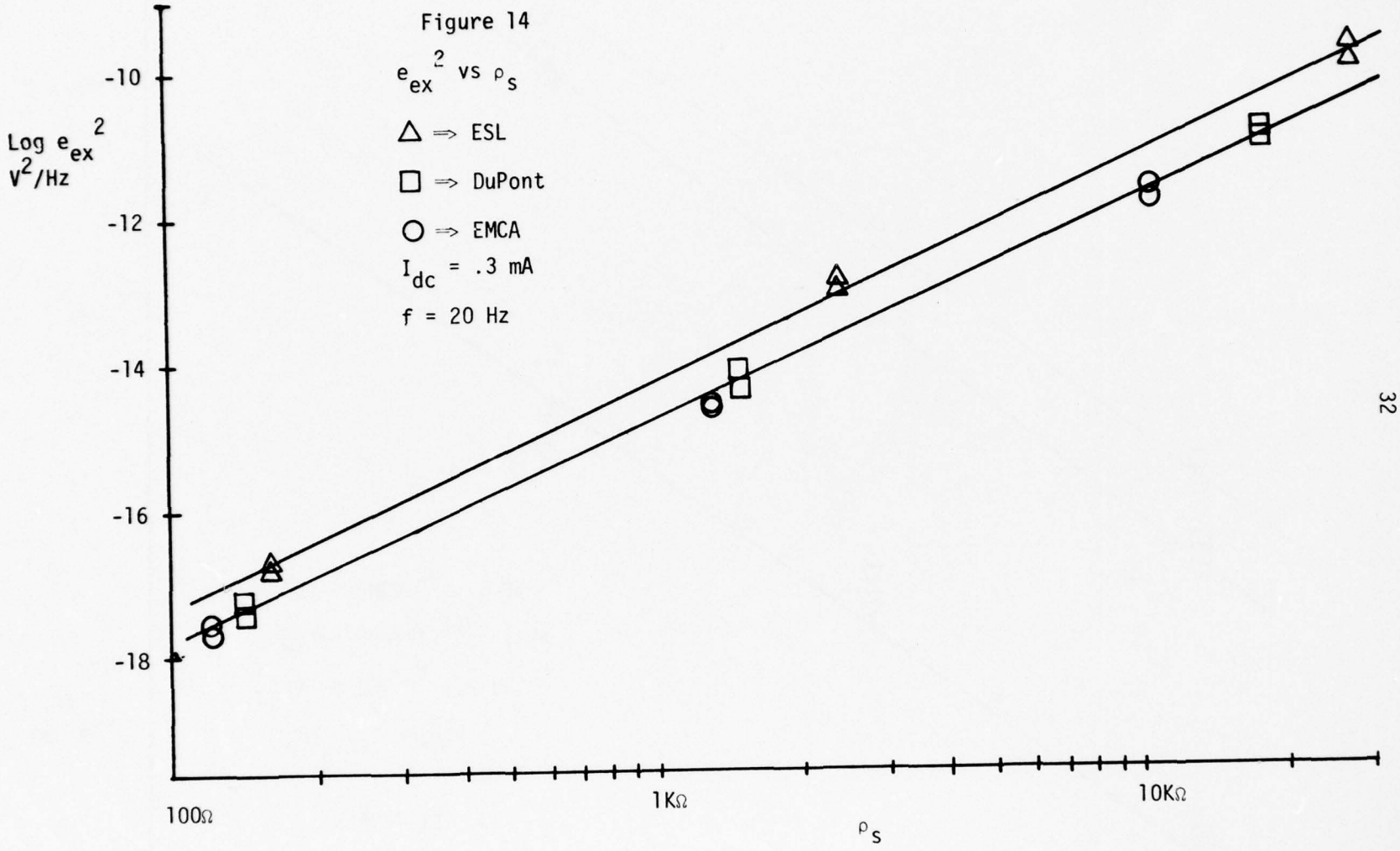
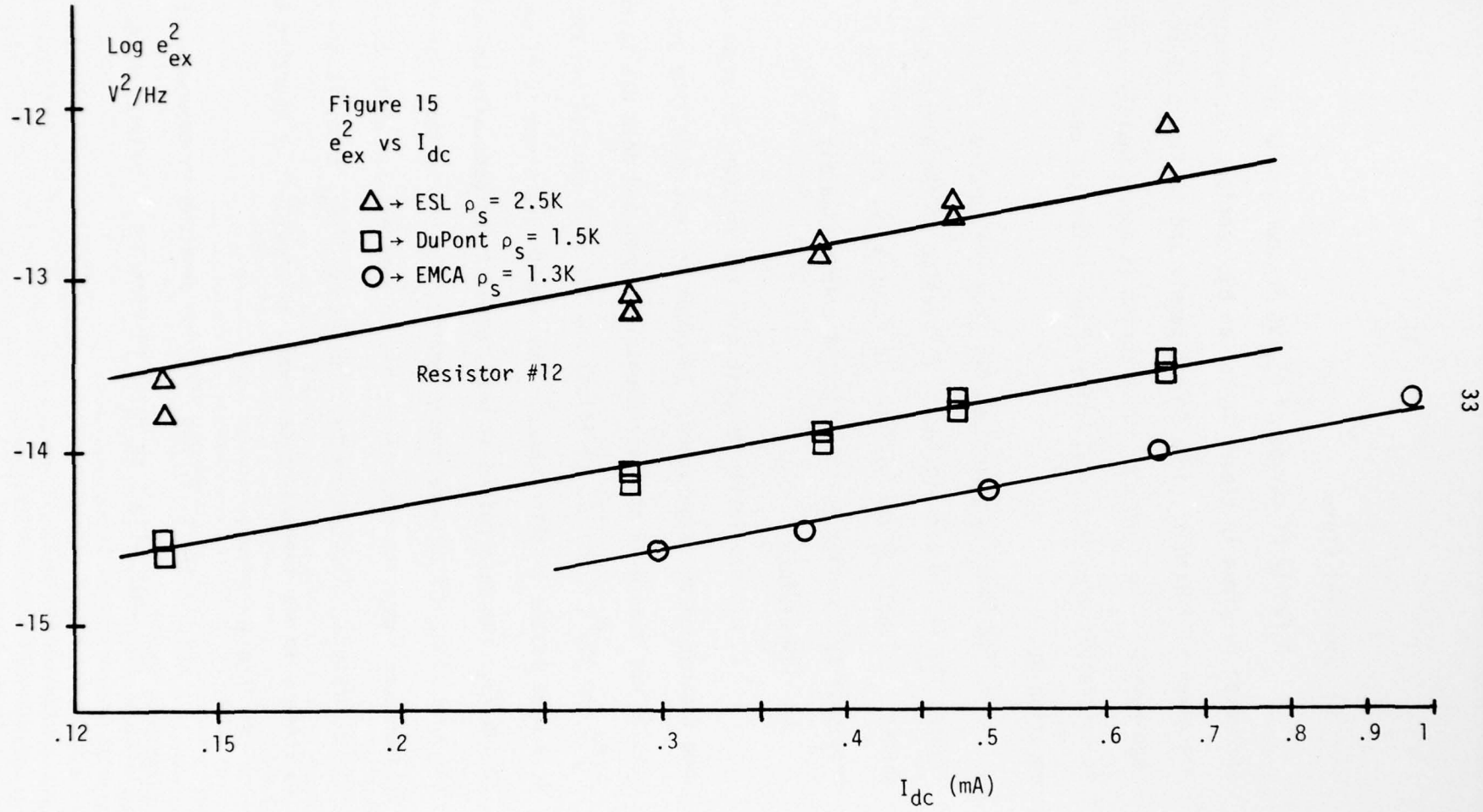


Figure 14
e_{ex}^2 vs ρ_s
△ ⇒ ESL
□ ⇒ DuPont
○ ⇒ EMCA
I_{dc} = .3 mA
f = 20 Hz
Log e_{ex}^2 V^2/Hz
-10
-12
-14
-16
-18
100Ω
1KΩ
10KΩ
ρ_s


Log e_{ex}^2
V^2/Hz
-12
-13
-14
-15
Figure 15
e_{ex}^2 vs I_{dc}
△ → ESL ρ_s = 2.5K
□ → DuPont ρ_s = 1.5K
○ → EMCA ρ_s = 1.3K
Resistor #12
.12
.15
.2
.3
.4
.5
.6
.7
.8
.9
1
I_{dc} (mA)

E) Spectral Plots

A family of curves of e_{ex}^2 vs frequency with Idc as a parameter is given in figure 16 for an ESL sample. Similar curves are given in figure 17 for a DuPont sample and in figure 18 for an EMCA sample. The slopes of these curves is approximately -1 which is consistent with the usual value of unity for the constant α in equation 5.

The break frequencies, f_B, from the spectral plots of figures 16, 17, 18 are plotted as a function of the electric field, E, across the length of the resistor in figures 19, 20, 21. As predicted by equation 6, the slopes are approximately 2.

F) Temperature

It was originally thought that the constant K' might exhibit some dependence on temperature. In order to test this, the probe station was placed in an environmental chamber and data was taken at $-35^{o}C$ and $+50^{o}C$. The ESL (iridium) and the EMCA (ruthenium) resistive inks were tested in this manner. The results are shown in figures 22 and 23. The data points at both temperatures generally coincide on the same line, within experimental error, indicating that over this temperature range the constant K' has no apparent 1st order dependence on temperature. The temperature dependence of f_B, then, is due entirely to changes in the thermal noise level, as predicted by equation 6.

G) Contact Effect

Two resistors, #7 and #14, are provided to determine the effect of TFR terminations on noise performance. Resistor #14A has seven

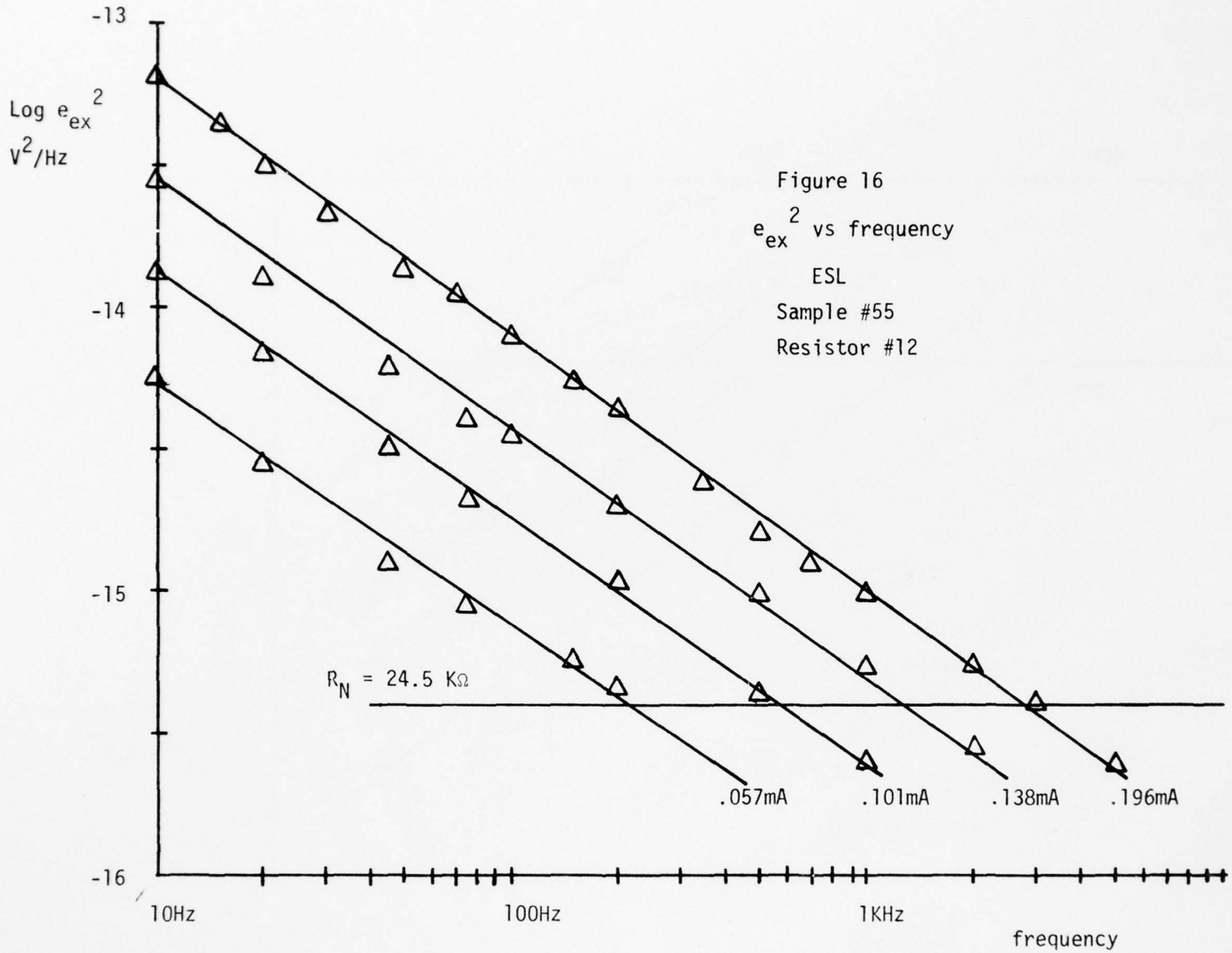


Figure 16

e_{ex}^2 vs frequency

ESL

Sample #55

Resistor #12

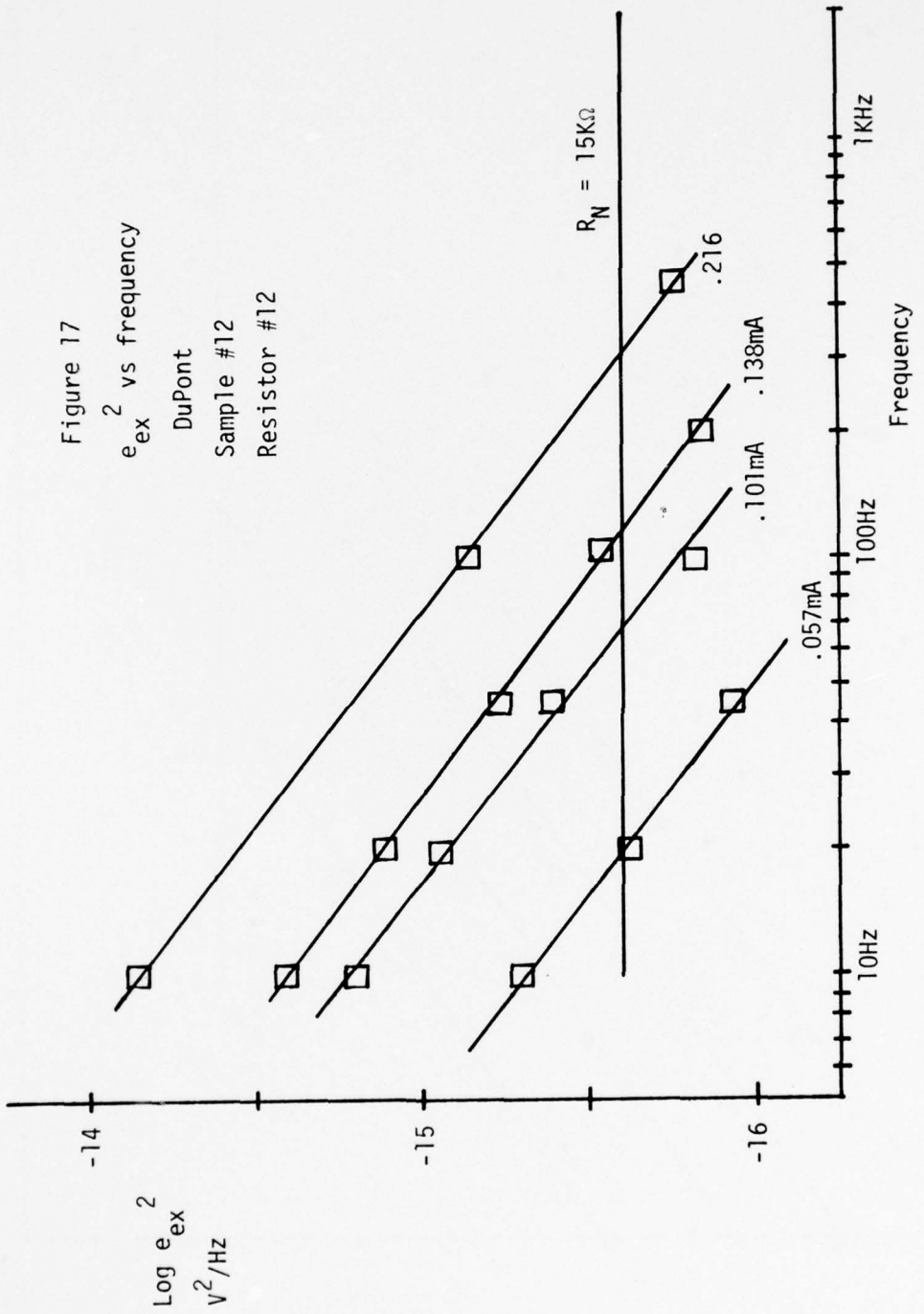


Figure 17
e_{ex}^2 vs frequency
DuPont
Sample #12
Resistor #12
R_N = 15KΩ
.216
.138mA
.101mA
.057mA
Log e_{ex}^2
V^2/Hz
-14
-15
-16
10Hz
100Hz
1KHz
Frequency

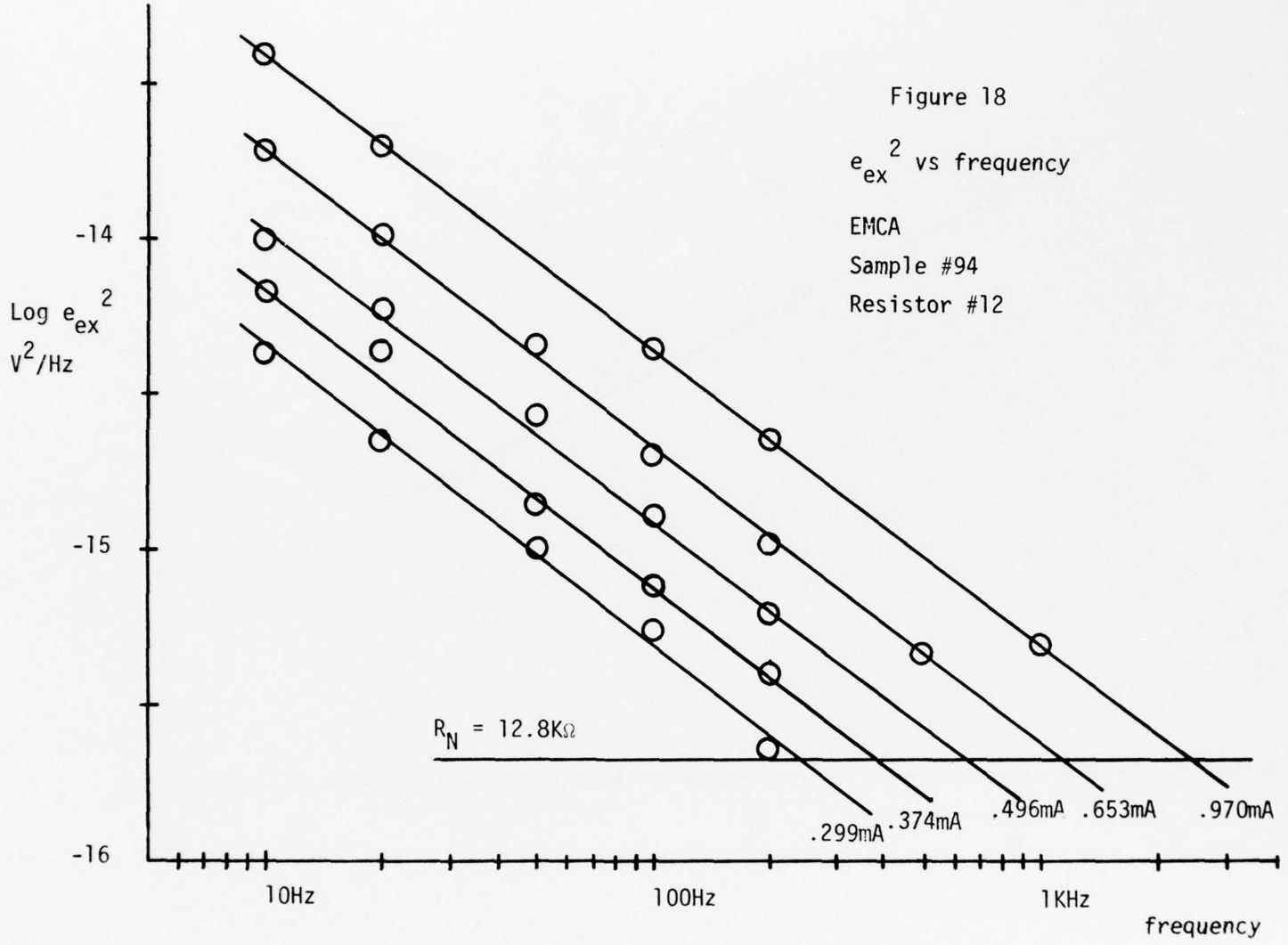


Figure 18

e_{ex}^2 vs frequency

EMCA

Sample #94

Resistor #12

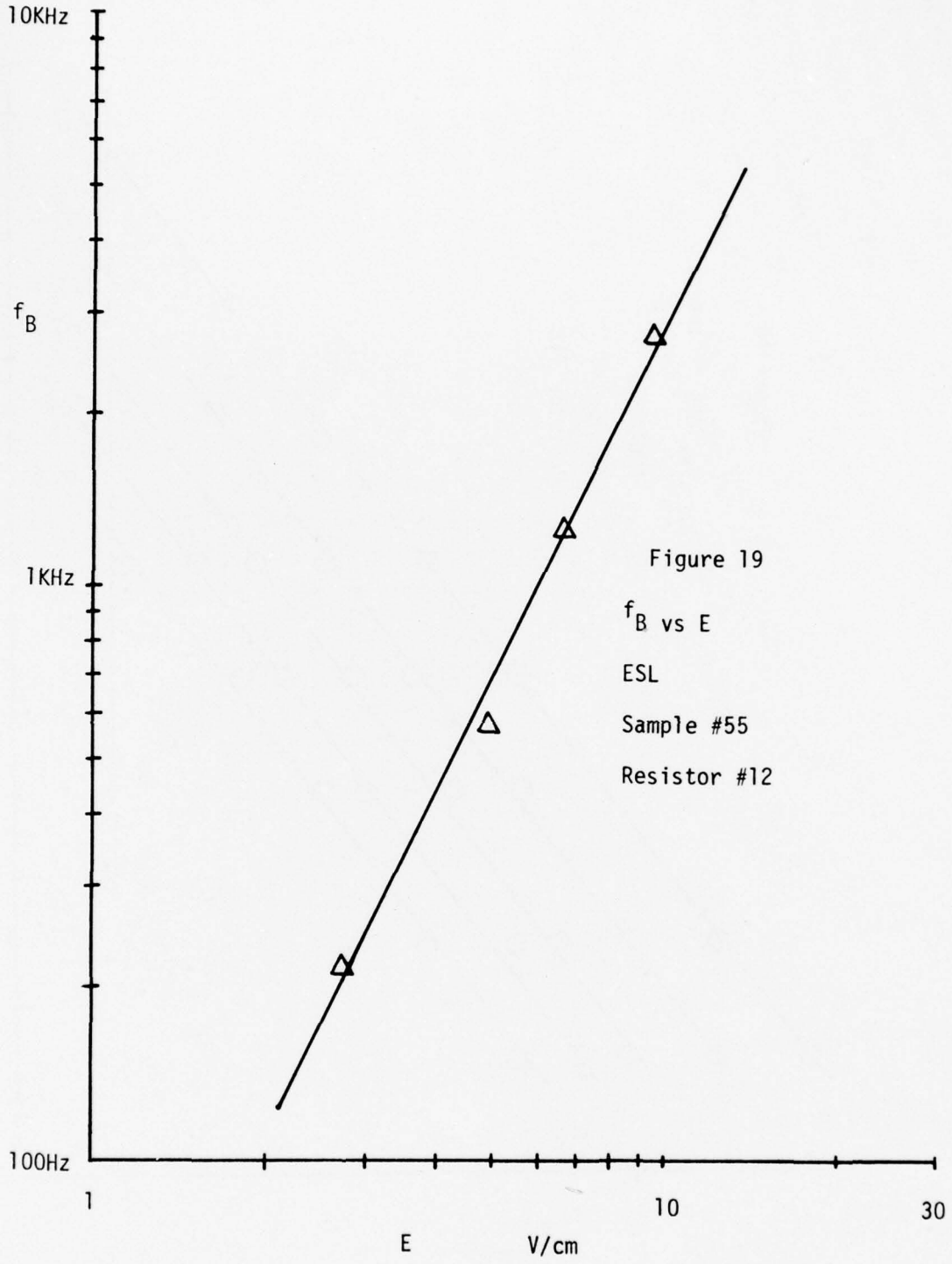


Figure 19

f_B vs E

ESL

Sample #55

Resistor #12

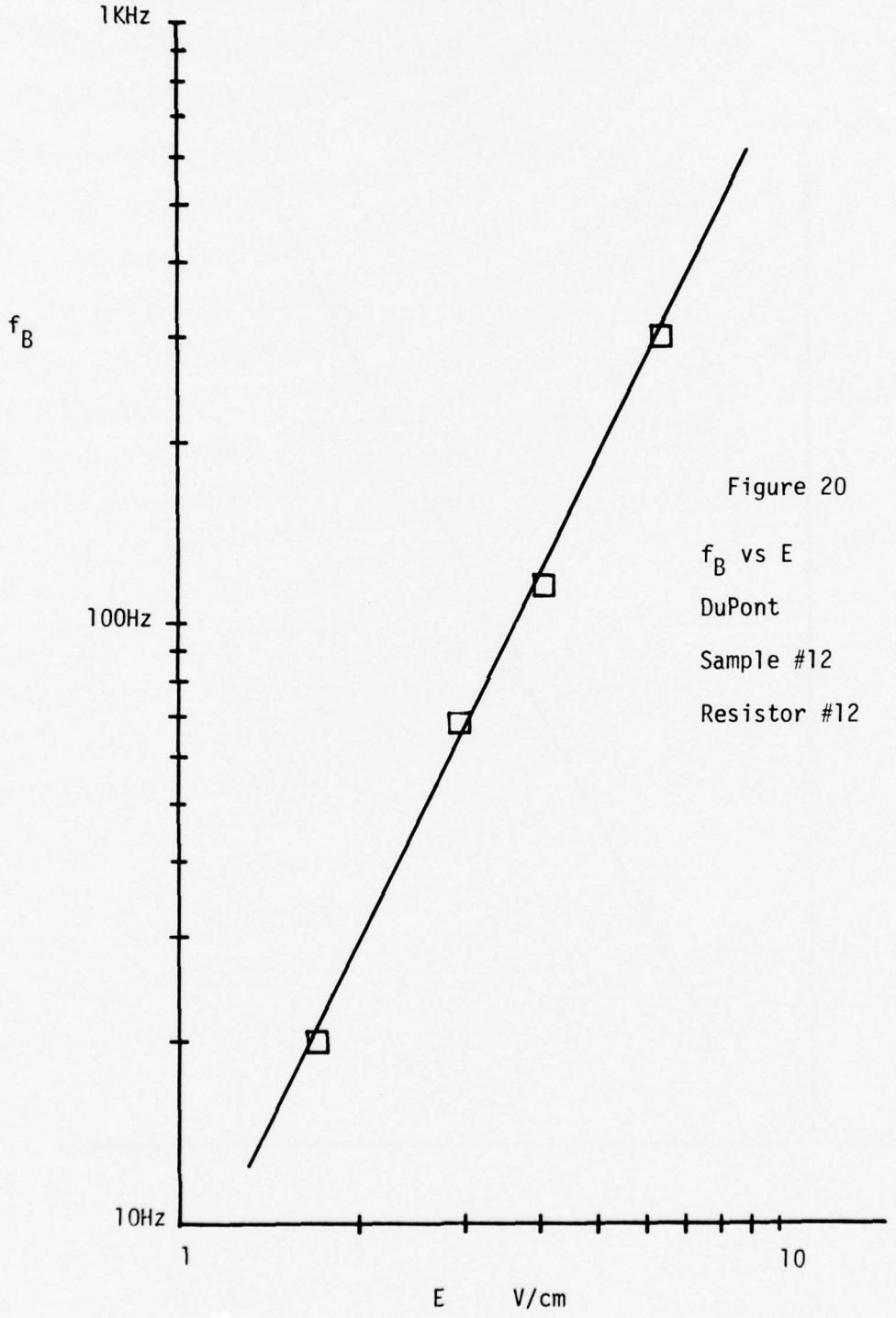


Figure 20

f_B vs E

DuPont

Sample #12

Resistor #12

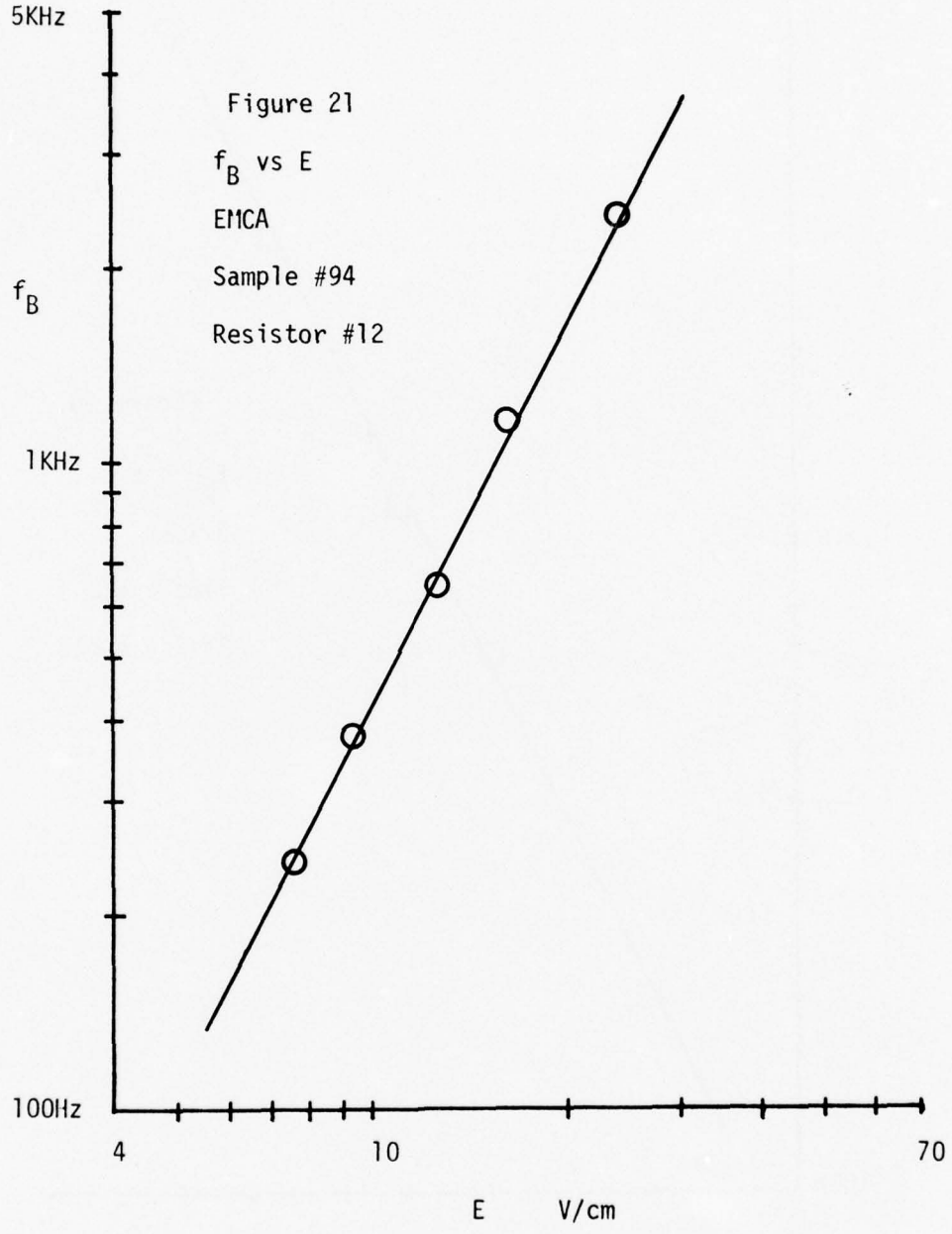


Figure 21

f_B vs E

EMCA

Sample #94

Resistor #12

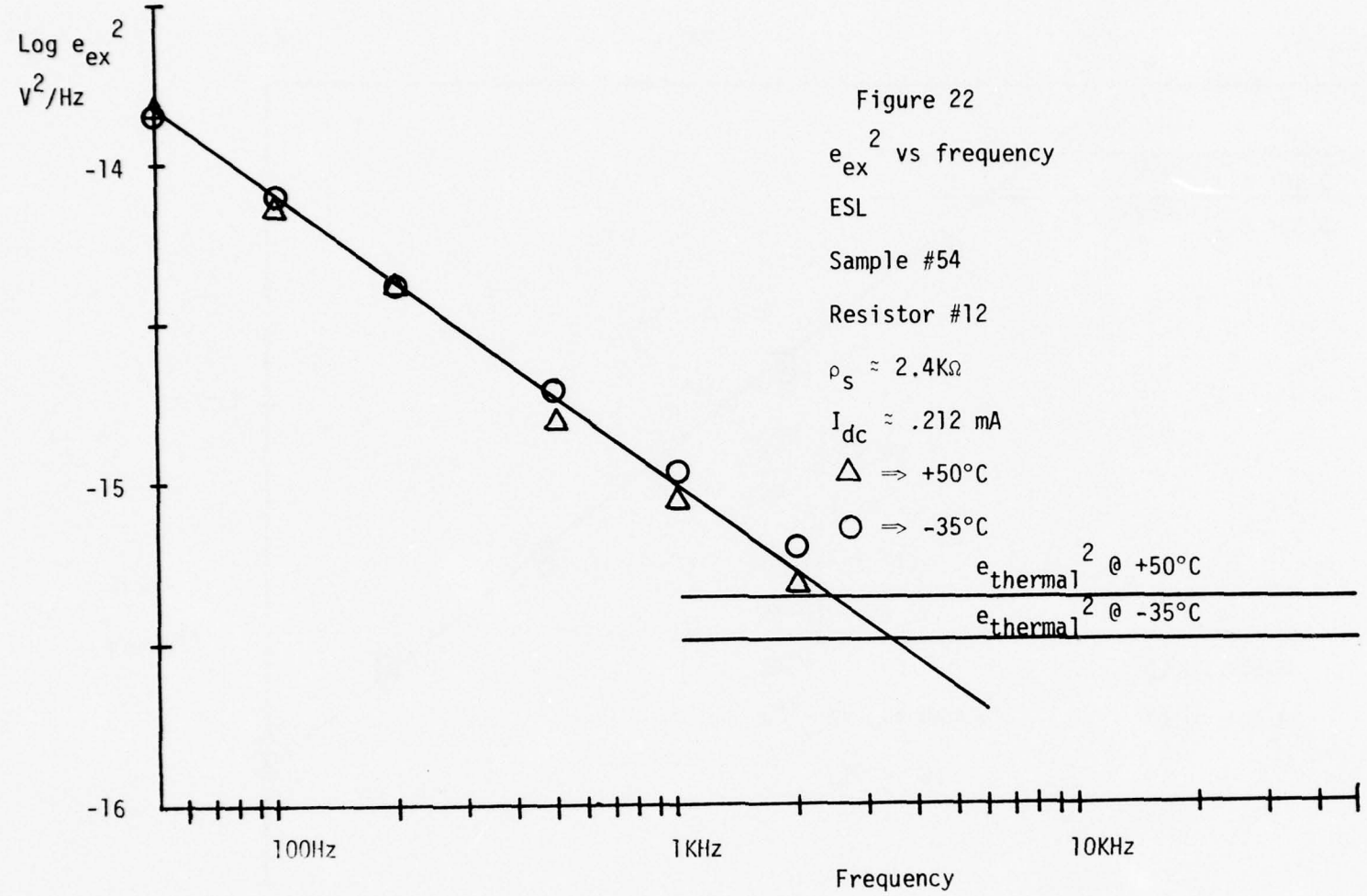


Figure 22

e_{ex}^2 vs frequency

ESL

Sample #54

Resistor #12

$\rho_s \approx 2.4K\Omega$

$I_{dc} \approx .212$ mA

△ ⇒ +50°C

○ ⇒ -35°C

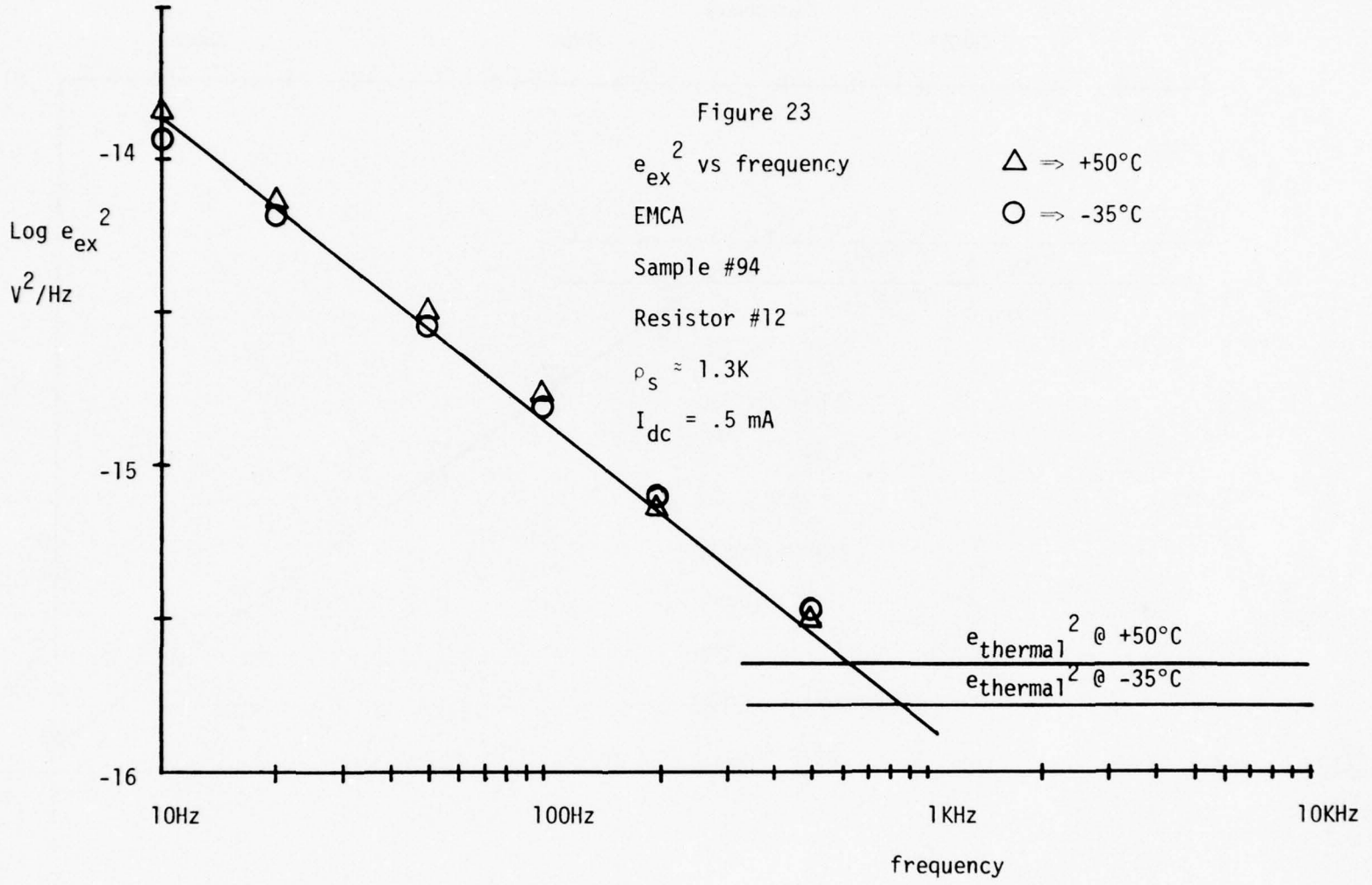


Figure 23
e_{ex}^2 vs frequency
EMCA
Sample #94
Resistor #12
$\rho_s \approx 1.3K$
$I_{dc} = .5$ mA
△ ⇒ +50°C
○ ⇒ -35°C
Log e_{ex}^2
V^2/Hz
-14
-15
-16
$e_{thermal}^2$ @ +50°C
$e_{thermal}^2$ @ -35°C
10Hz
100Hz
1KHz
10KHz
frequency

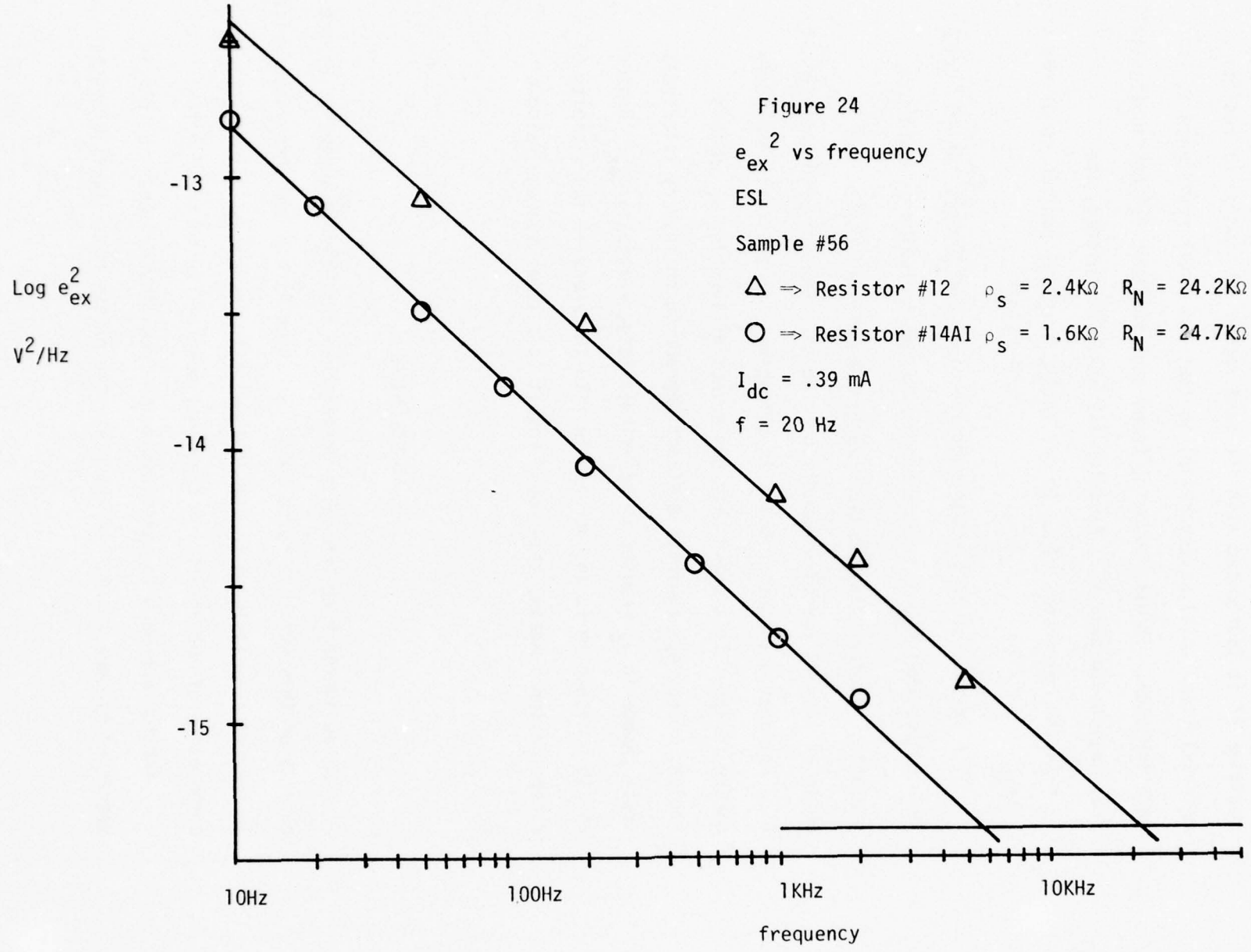


Figure 24

e_{ex}^2 vs frequency

ESL

Sample #56

△ ⇒ Resistor #12 ρ_s = 2.4KΩ R_N = 24.2KΩ

○ ⇒ Resistor #14AI ρ_s = 1.6KΩ R_N = 24.7KΩ

I_{dc} = .39 mA

f = 20 Hz

extra contacts fabricated serially in the body of the resistor, while resistor #7 is fabricated with the same number of squares of resistive material (same total aspect ratio) so that the total resistance is the same for each. It was, however, found that resistor #14 has substantially less resistance than #7. Resistor #12 was used instead, its R_N = 24.2KΩ being very close to the 24.7KΩ terminal resistance of resistor #14AI.

The results of this experiment are given for the ESL ink in Figure 24. Notice that e_{ex}^2 has been reduced by the inclusion of the extra contacts. At least two possible mechanisms may be responsible in whole or in part for this reduction in noise. Possibly, in the vicinity of a termination, contact metal is diffusing into the resistive paste during firing. This would have the effect of lowering ρ_S in this region. Since e_{ex}^2 exhibits a direct dependence on ρ_S^3, any relatively small change in ρ_S results in relatively large change in e_{ex}^2. Another possible mechanism is an increase in film thickness in the vicinity of a termination. Again, this would result in a lower average value of ρ_S.

V. CONCLUSION

A new approach to TFR noise performance analysis is suggested by the results of this work. A noise model (equation 5) has been presented which is specifically tailored to use in thick film technology. It allows the computation of the entire low frequency spectral response of a TFR.

Another approach to optimization of frequency response in TFRs is suggested by equation 6. In the past, the excess noise level of resistors

in the low frequency region of the spectrum has often been of such a magnitude that designers considered the entire noise response to be of a 1/f nature. However, as can be seen in the spectral plots presented, in modern high performance, low frequency circuits, the TFR's noise break frequency, f_B, may fall within the low frequency region or the region of interest. Since the thermal noise level places a fundamental lower limit on noise performance, maximum noise performance optimization is achieved when f_B is placed below the frequency band of interest. Equation 6, then gives the designer a powerful tool for TFR noise optimization; any parameter change which reduces the electric field, E, across the length of the TFR will lower f_B a proportional amount.

Use of either equation 5 or 6 requires only the determination of a single constant, K′, for a given resistive ink. K′ has been shown, to a first order approximation, to be a property only of the resistive material and firing conditions and is independent of the various TFR parameters over the ranges tested. From the data presented, values of K′ may be computed for each of the three resistive pastes. Caution is advised on the use of equation 5 for this computation. Using equation 5, values of K′ computed for a given ink from various data curves were found to vary by as much as an order of magnitude. Except for normal scatter in data, this was found to be largely caused by the fact that the actual ρ_S differed, in some instances, by as much as a factor of about 2.5 from the nominal value. Whether this is caused by variation in bulk resistivity or print thickness from their nominal values could not be determined.

A more accurate determination of K′ is achieved by use of the e_{ex}^2 vs E^2 data curves and equation 6, where ρ_S and other factors have been absorbed into the E term, which is easily determined. The following approximate values for K′ were obtained from this calculation:

ESL - 5×10^{-19} mho-cm^2

DuPont - 1.3×10^{-19} mho-cm^2

EMCA - 7×10^{-20} mho-cm^2

Since the constant K′ offers an index for comparison of relative noise performance, it is interesting to note that the two ruthenium based inks (DuPont and EMCA) exhibit superior noise performance over the iridium based (ESL) ink.

TFR terminations have been demonstrated to have a significant effect on noise performance for the ESL resistor/conductor ink system. Two possible mechanisms for this phenomena have been presented, but the means to prove or disprove either was not available. Available time precluded the testing of the other two ink systems for this same phenomena.

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Part 6

NOISE IN OPTICAL ISOLATORS

Prepared for

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I. INTRODUCTION

The purpose of this work is to investigate the noise behavior of the optical-isolators. Investigations on the terminal noise behavior of the optical-isolators have been made, so that a comparison between the noise behavior of the optical-isolators and that of the conventional bipolar transistors can be made. The contribution of noise due to the light emitting diode and the phototransistor will be analyzed. Investigation concerning the noise behavior of the optical-isolators will give an evaluation of the LED biasing used in optical-isolators. Noise in low frequency region is emphasized. Both burst noise and excess noise are examined. Finally, a noise model for the optical-isolators will be constructed, so that the noise behavior of the optical-isolators can easily be determined in terms of measurable parameters.

II. OPERATION OF OPTICAL-ISOLATORS

The optical-isolators can be divided into several types. The devices to be investigated in the task are those with a ligh emitting diode (LED) as input device and a phototransistor as output device.

The devices used in the experiment were from different manufactures, but all with the same construction. A gallium arsenide infrared light emitting diode and a silicon phototransistor are mounted together in a dip package to form an optical-isolator. When forward current I_D is passed through the Gallium Asenide Diode (LED) it emits infrared radiation. The radiation energy is transmitted through an optical medium and falls on the surface of the phototransistor. The phototransistors are designed to have a large base area and a small emitter area. Some fraction of the photons due to radiation strike the base and cause the generation of electron-hole pairs. For NpN phototransistor, high electric field across the collector base junction draws the electrons into the collector. The common circuit configuration is to leave the base floating. With this connection, the holes generated in the base region will cause the base potential to rise, thus forward biasing the emitter base junction. Electrons are then injected into the base from the emitter trying to neutralize the excess holes. Because of the close proximity of the collector junction and high electric field between collector and base. Most of the electrons are swept into the collector region. As a result, the collector current is much higher than the photogenerated current, thus providing a current gain.

Although the optical-isolator is not originally designed as a linear device, with a proper choice of LED forward current I_D, it does give a wide range of linear operation. Figure 1 shows the transfer relation between I_D and I_C. Over quite a wide range, I_C can be

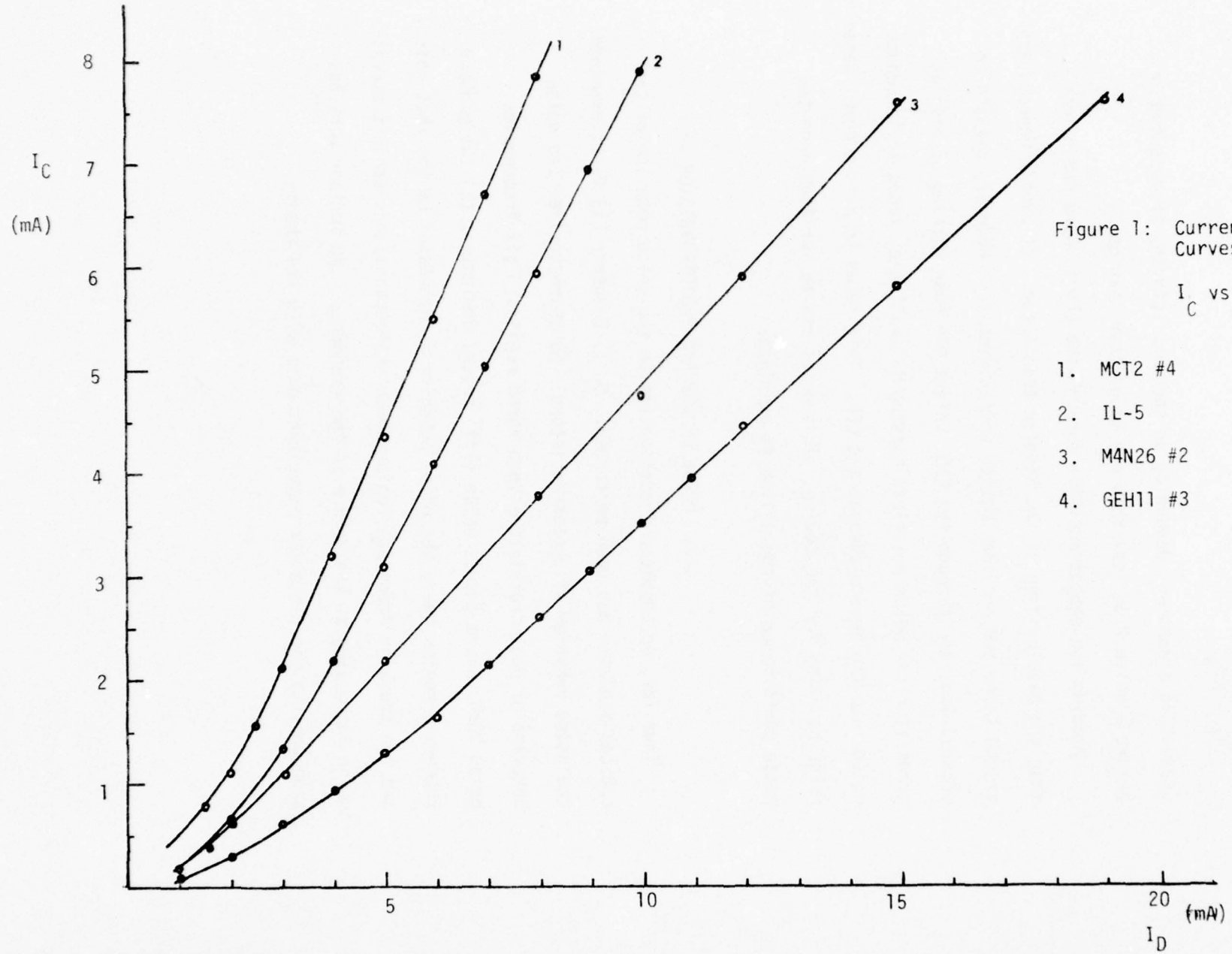


Figure 1: Current Transfer Curves

I_C vs I_D

1. MCT2 #4
2. IL-5
3. M4N26 #2
4. GEH11 #3

expressed as

$$I_C = KI_D$$

where K is a constant depending on the manufacturing process and may assume a value from less than one to greater than one.

Biasing the phototransistor through the LED is more convenient than the base biasing of the bipolar transistor. It avoids unnecessary ground loops and provides better noise immunity. However, biasing the optical-isolator through the LED, unlike the base biasing of bipolar transistor for which noiseless biasing is available, tends to introduce noise into the device through the LED. This leads to a more complicated noise behavior for the device. This point can be verified once the noise performance of the device is examined.

III. NOISE OF LED AND PHOTOTRANSISTOR

Thus far, no complete investigation on the noise behavior of the optical-isolator has been performed. G. T. Daughter [1] first examined the noise behavior of phototransistors. He characterized the noise behavior of phototransistors into three regions; (1) frequencies below $10kH_z$ where excess noise ($1/f^{\alpha}$ noise) dominates, (2) the midband frequency region where the noise behavior is dominated by the shot noise, and (3) the high frequency region where phototransistors exhibit excess noise increasing as the square of the frequency. No further work has been done to correlate the experiment data with the theory.

De La Moneda [2] investigated the noise in phototransistors and constructed a simple model. He derived the expression for dc current flowing across the emitter and collector junctions with base floating, then used the expression to obtain the corresponding shot noise generator that is located across the device junction. The noise of the photodiode of the phototransistor was treated as a shot noise generator. His model for phototransistors is good only for high frequencies; low frequency noise behavior was not explored in his work.

Noise behavior of the LED was also investigated by T. P. Lee [3], Jean Conti and others [4]. In Lee's work, experiments were performed on GaAs diodes and (Al-Ga) As diodes under high current densities. The results revealed that the LED's investigated showed $f^{-\alpha}$ noise behavior at low frequencies with α less than unity. Jean Conti investigated the intensity fluctuation of GaAs LED at room temperature. His work concerning the $f^{-\alpha}$ noise behavior of LED's revealed the dependence of α on LED currents.

As was mentioned above, the LED itself might exhibit undesirable levels of noise especially when the device is used in low noise application where low frequency noise is an important design criteria. Since the optical-isolator is composed of an LED and a phototransistor, it is clear that the noise behavior of optical-isolators be a combination of both of the LED and the phototransistor.

IV. TWO DOMINANT LOW FREQUENCY NOISE SOURCES

For most active devices, the low frequency noise behavior is dominated by two noise sources, excess noise and burst noise.

Many have investigated the existence and physical origins of these two types of noise sources. Different investigators have approached the problem from different points of view and have arrived at different conclusions.

A) Burst Noise

Burst noise has been found in resistors, reverse biased or forward biased p-n junctions, operational amplifiers, transistors and optical-isolators. Burst noise appears as telegraph-type, randomly distributed dc level shift. It has equal amplitude but different pulse widths. The pictures attached on the back show the burst noise that was found in optical-isolators. Both bistable and multistable level burst pulses may exist in devices with burst noise. The power spectrum of bistable burst noise is of $f^{-\alpha}$ form with $1<\alpha<2$. A refined form of its current spectrum can be expressed as [5]

$$I_{BN}^2 = \frac{K_1 I \Delta f}{1+\pi^2 f^2/4a^2}$$

where K_1 is a constant and a represents the number of burst/sec.

The existence of burst noise will significantly affect the noise behavior of the device. Many have investigated the functional dependence of burst noise on current, voltage and temperature. Physical mechanism for burst noise has been searched for, but

so far no unique answer or model can satisfactorily explain all the behaviors of burst noise.

Card and Chaudhari [6], after investigating the reverse biased germanium p-n junctions, tunnel diodes and carbon composition resistors, found that burst noise may exist in such components and suggested that the burst noise was due to surface breakdown.

In D. Wolf and E. Holler's work [7], it was found that when the base to emitter junction of the p-n-p transistor was reverse biased far below breakdown, the transistor would show bistable fluctuations.

Leonald and Jaskolski [8], in their observation of the burst noise in the reverse biased collector and base junctions, relate the phenomenon of burst noise to the negative region of the collector and base V-I characteristics.

In Knott's work [9], results showed that the burst noise may exist in forward-biased emitter and base junctions with collector floating.

A burst noise model for forward-biased p-n junction diodes was first constructed by Hsu and Whitter [10]. It proposes that burst noise results when the current through a defect is modulated by a change in the charge state of a single generation-recombination center located adjacent to the defect. Both the burst amplitude and pulse width are related to the basic properties of the generation-recombination center and the defect.

Cook and Brodersen [11] extend Hsu and Whitter's work of burst noise to include sources of burst noise in bulk material and at the surface. They indicate several locations of crystallographic defects which can

lead to burst noise. The locations are the bulk emitter-base space charge region, base surface and the area of the emitter-base space charge region at the surface.

In Oren's correspondence [12], different views on the burst noise were compared, conflicting ideas about the burst noise were mentioned. It was indicated that burst noise was due to many factors, such as surface problem, metal precipitate, dislocation of crystal lattice and so on. No unique explanation can properly account for all the behaviors of burst noise.

It must be pointed out here that since burst noise can be found in forward biased diodes, the use of the LED in biasing the optical-isolator will inevitably increase the possibility of significant burst noise in such devices. The results of the measurments on the noise of the optical isolators will verify this point.

B) Excess Noise (1/f noise)

Excess noise will dominate the low frequency noise behavior in the absence of burst noise. It is found in most electronic devices, such as tubes, transistors, diodes and resistors. An excess noise power spectrum has an $f^{-\alpha}$ form with α between 1 and 2. In most cases, α is close to unity.

The origin of excess noise in transistors was explained by Fonger [13] as a phenomenon of fluctuation in current combining at the base surface. Sah and others [14] have shown experimental evidence supporting the surface noise theory.

Gibbons [15] suggested that in low noise transistors the principal source of excess noise may be in the emitter and base transition region instead of on the base surface.

R. C. Jager and A. J. Brodersen [16] indicated that more than one 1/f noise sources may exist in silicon planar transistors and indicated their proper locations in the transistor noise model. They indicated that one 1/f noise is due to surface recombination which is affected by the inactive base resistance. The other 1/f noise is due to the recombination in the vicinity of the active region which is affected by the entire base resistance.

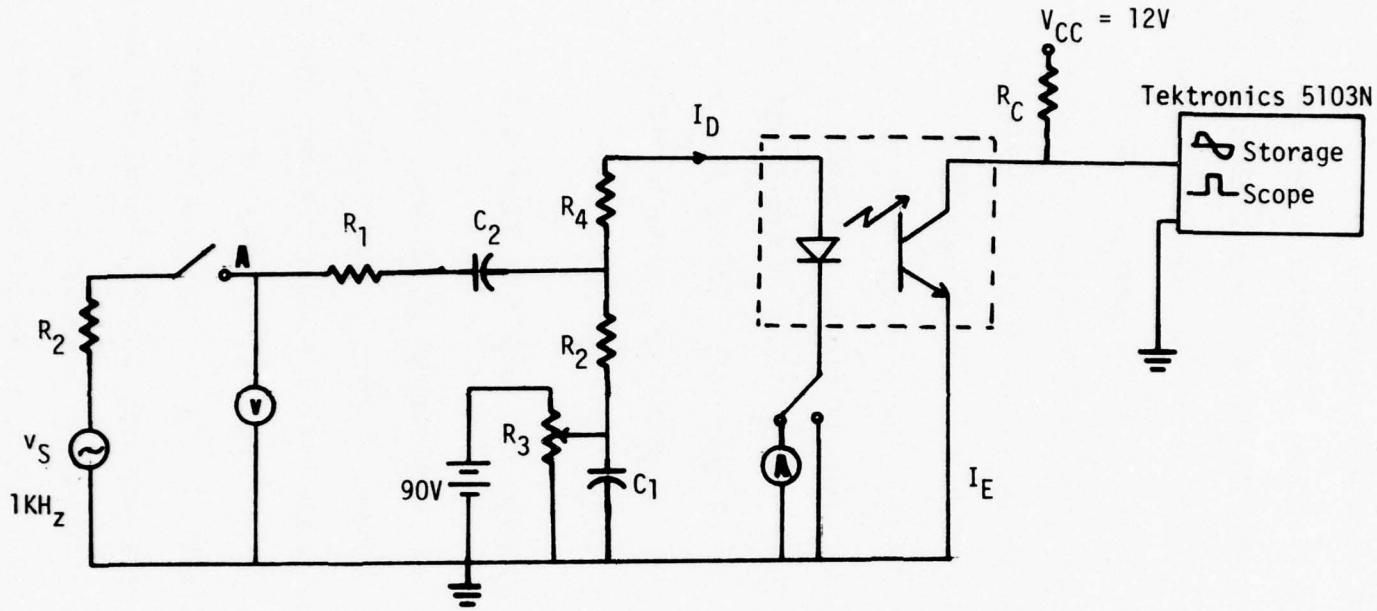
In order to investigate the noise behavior of the optical-isolators, a total of about twenty optical-isolators from different manufactures were used. Devices with clean burst noise and a higher rate of incidence were examined separately. Devices that do not show conspicuous burst noise for direct burst noise amplitude measurement were investigated by their noise spectrums.

V. MEASUREMENT TECHNIQUE AND RESULTS OF BURST NOISE

Burst noise measurement is approached in two ways. One is to examine the functional dependence of burst occurence rate, pulse width and pulse amplitude on the biasing voltage, biasing current and temperature. The other is to examine its noise spectrum.

A Fairchild 820-527 optical-isolator with clean and high incidence rate of burst noise was used in the following experiment.

The schematic circuit diagram for measuring the burst noise is shown in Figure 2. The LED of the optical-isolator is biased with



on the scope:

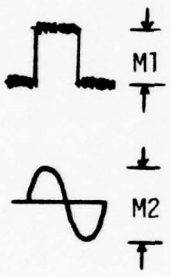


Figure 2: Schematic Diagram for Measureing Burst Noise Current Amplitude.

R_1 = 10.21KΩ

R_2 = 97Ω

R_3 = 50KΩ

R_4 = 1.9KΩ

C_2 = 100μF

C_1 = 3500μF

R_C = 970Ω

a constant current source. A ten-turn wire-wound potentiometer is used in adjusting the desired LED forward current I_D. All capacitors are large enough so that they appear as AC short-circuited and do not affect the frequency response of the system. Because the amplitude of the burst can not be adequately measured with a volt meter, a Textronics 5103 N storage scope (calibrated) was used to measure the burst noise on the scope. The burst noise was stored on the scope and its voltage amplitude M1 was measured. By injecting a $1kH_z$ sine wave signal from terminal A and ground with RMS voltage V, a sinewave output was again measured on the scope giving a peak to peak voltage M2. The equivalent burst noise current amplitude reflected to the LED can be calculated as

$$I_{BN} = 2.828 \frac{(\frac{M1}{M2})\ R2}{(R_1+R_2)\cdot(R_2+R_4)} \quad .$$

A mathematical derivation is given in Appendix 1. The dependence of burst noise I_{BN} on LED current I_D is shown in Figure 3A. The dependence of I_{BN} on I_E is also shown in Figure 3B. I_{BN} can be expressed as a function of I_D,

$$I_{BN} = k_1 I_D^{N_1} \quad , \qquad N_1 = 0.36 \ , \tag{1}$$

where $k_1 = 41.3$ uA.

Figure 3A: Dependence of I_{BN} and δI_C on I_D.

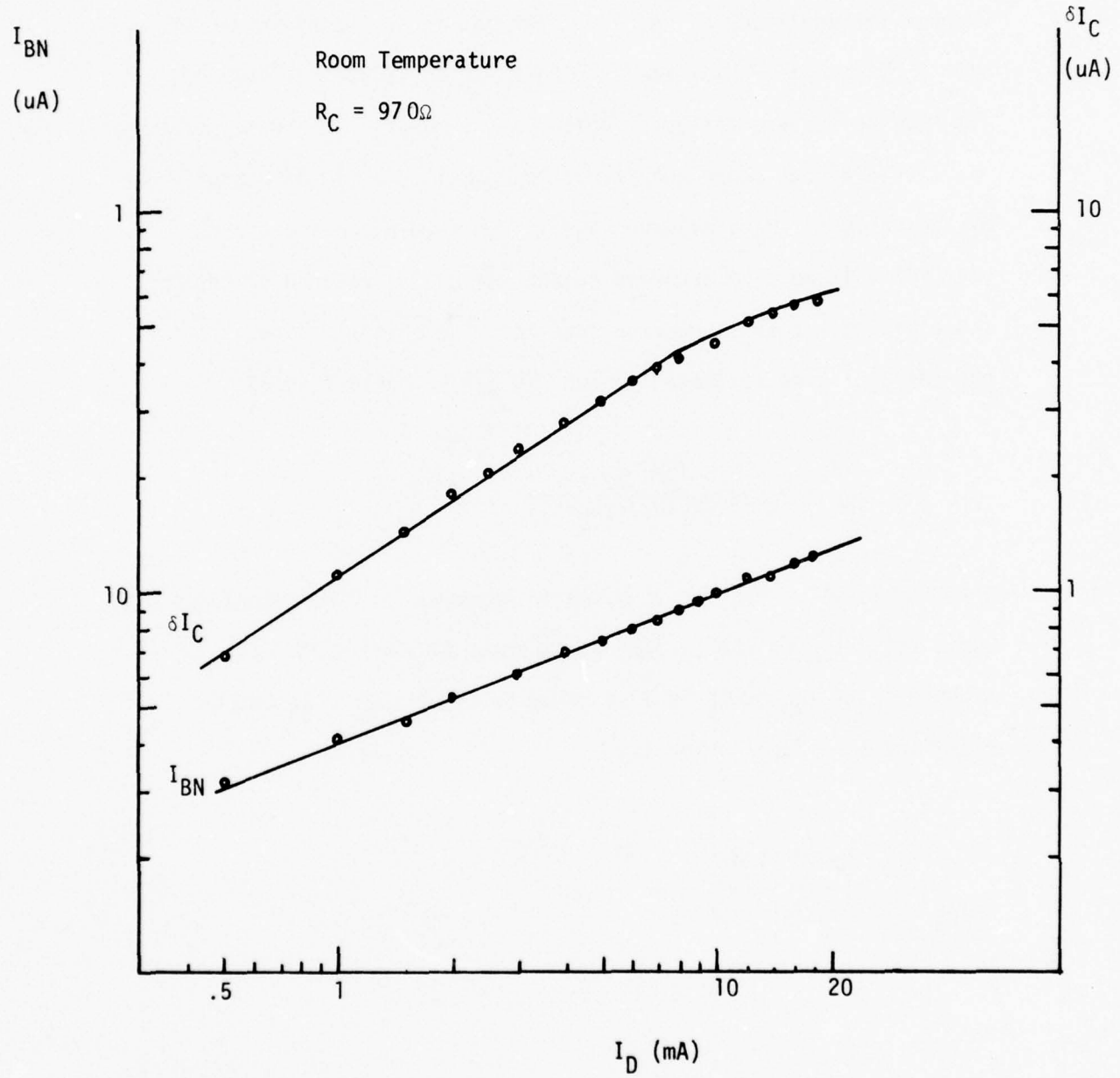
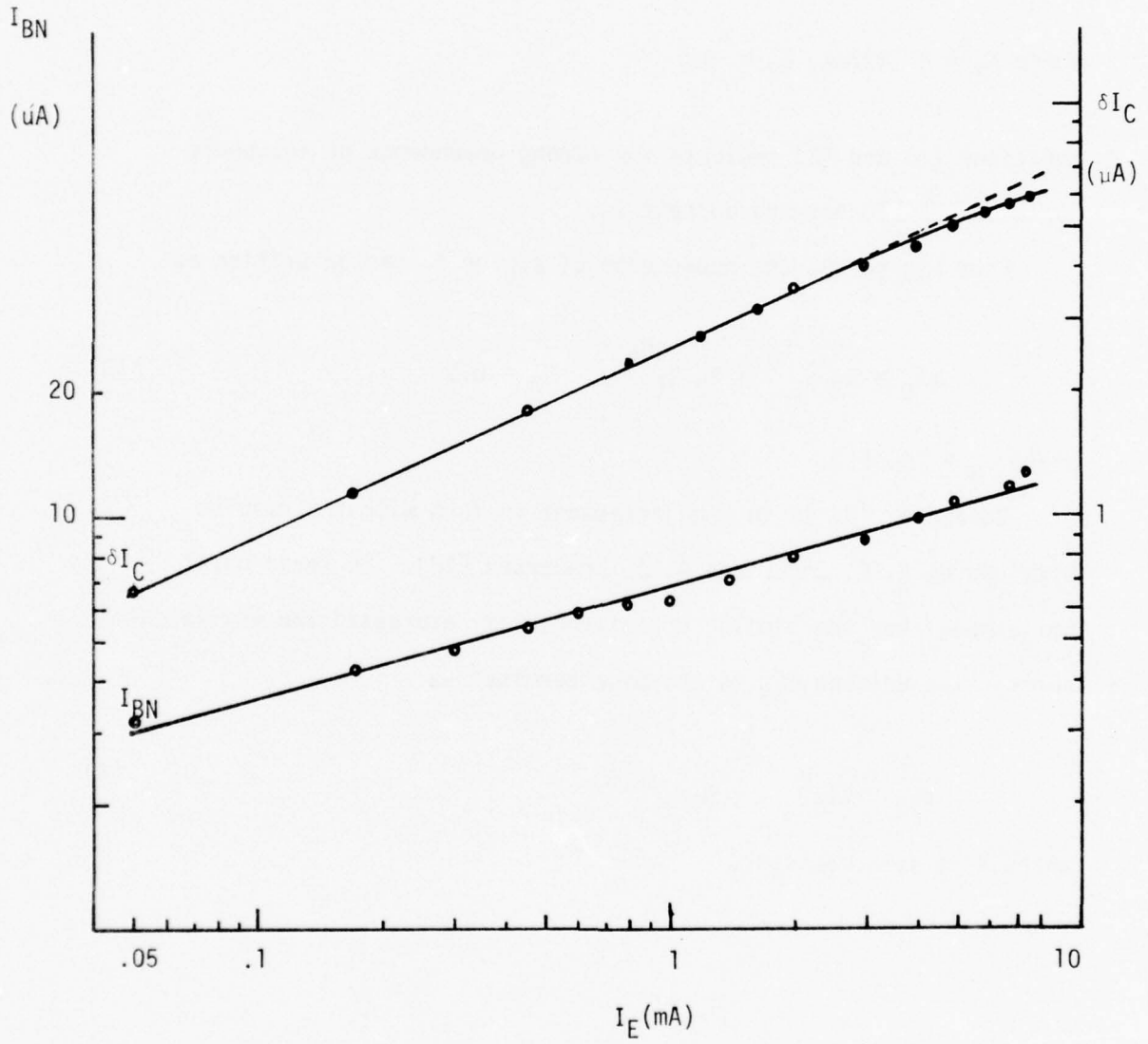


Figure 3B Dependence of I_{BN} and δI_C on I_D.

Room Temperature

R_C = 970Ω



If we define the output burst noise current at the collector of phototransistor as

$$\delta I_C = \frac{M1}{R_C}$$

then the dependence of $\delta 1_C$ on I_D can be expressed as

$$\delta I_C = K_2 \, I_D^{N_2} \tag{2}$$

where $K_2 = 0.1327\text{mA}$, $N_2 \doteq 0.7$.

Equations (1) and (2) indicate the strong dependence of the burst noise on the LED forward current I_D.

From Figure 3B, the dependence of δI_C on I_E can be written as

$$\delta I_C = K_3 \, I_E^{N_3} = K_3 \, I_C^{N_3}, \quad N_3 \doteq 0.5 \tag{3}$$

where $K_3 = 75.59\text{uA}$.

Equation (3) is in good agreement in form with the results obtained by R. C. Jager and A. J. Brodersen [16]. In their burst noise model for the bipolar transistor, they expressed the equivalent burst noise voltage E_{BN} to the base terminal as

$$E_{BN} = KI_C^{N}, \quad N \doteq 0.5 \tag{4}$$

where K is some constant.

The burst noise model constructed by them is shown in Figure 4. In the optical-isolator, the base is floating, Figure 4A can be modified into Figure 5, with

$$E_{BN} = I_{BN} (\gamma d + \gamma \pi) = K I_C^{N} . \tag{5}$$

From Equation (2) and (3), an expression for I_C in terms of I_D can be written as

$$I_C = \left[\left(\frac{K_2}{K_3}\right) I_D^{N_2} \right]^{\frac{1}{N_3}} = K' I_D^{N'} \tag{6}$$

where $K' = \left(\frac{K_2}{K_3}\right)^{1/N_3}$, $N' = \frac{N_2}{N_3}$.

Inserting Equation (6) into Equation (5), we have

$$E_{BN} = K(K' I_D^{N'})^N \tag{7A}$$

Equation (7A) can be simplied, by inserting into the values of K′ and N′, as

$$E_{BN} = K[3.08 \ (I_D)^{1.4}]^N \tag{7B}$$

Equation (7B) expresses the burst noise voltage for the optical-isolator in terms of LED currents and some constants that can be determined by measurements.

Work on burst noise is not finished and will be continued in the future.

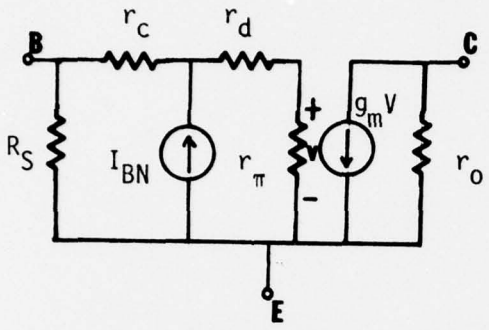


Figure 4A

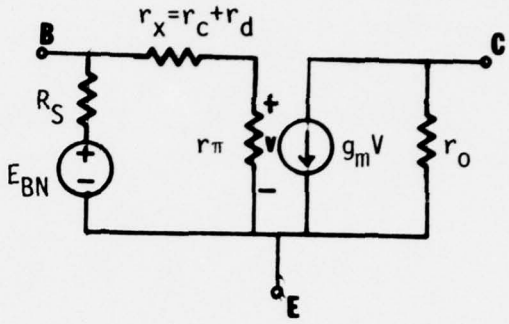
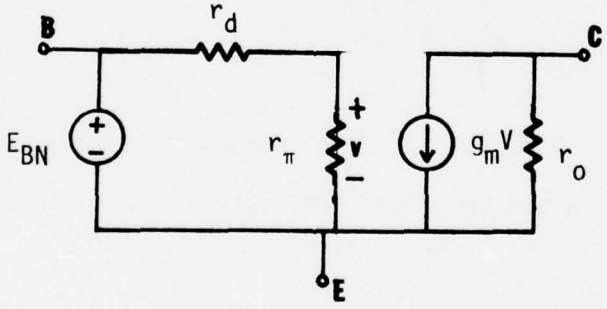


Figure 4B

$$E_{BN} = K(I_C)^N$$

$$N \pm 1/2$$



$$R_S = \infty$$

$$E_{BN} = K(K' I_d^{N'})^N$$

Figure 5 Burst Noise Model for Optical-Isolator with Base Floating.

IV. MEASUREMENT TECHNIQUE AND RESULTS FOR LOW FREQUENCY NOISE

The devices without large burst noise were investigated. Figure 6 shows the experiment set up. Measurements of the equivalent input noise voltage spectrum were performed using a combined technique of sinewave method and noise generator method. The equivalent noise input of the low noise preamplifier is very low over the frequency range of measurement, so that the noise of the preamplifier can be neglected in the calculation of equivalent input noise voltage spectrum E_N. Load resistor R_C of the optical-isolator was chose so that the phototransistor was operating in the active region and not loaded by the input impedance of the preamplifier. Mathematical derivation of the equivalent input noise voltage is shown in Appendix 2.

Figure 7A shows some spample noise voltage specturms for the devices with relatively low LED current I_D. Figure 7B shows some of the noise spectrums for devices with relatively high I_D. Comparisions between figure 7A and figure 7B reveal that for the case of high I_D, there are distinct break frequencies in the low frequency region, while for the case of low I_D, break frequencies are not so distinct.

As was mentioned in Part II, the biasing of the phototransistor was set by the LED. It is possible that high current densities in the LED will cause more noise through surface recombination, lattice dislocation and other mechanisms that affect the total noise behavior of the optical-isolator. Data is not yet available to verify this conjecture.

Figure 6: Schematic Diagram for Measuring Equivalent Input Noise Voltage of Optical-isolators.

R_1 = 1KΩ

R_2 = 1.9KΩ

R_3 = 51.7Ω

R_4 = R_5 = 50Ω

C1 = C2 = 100μF

R_D Wire Wound Resistor

R_C Metal Film Resistor

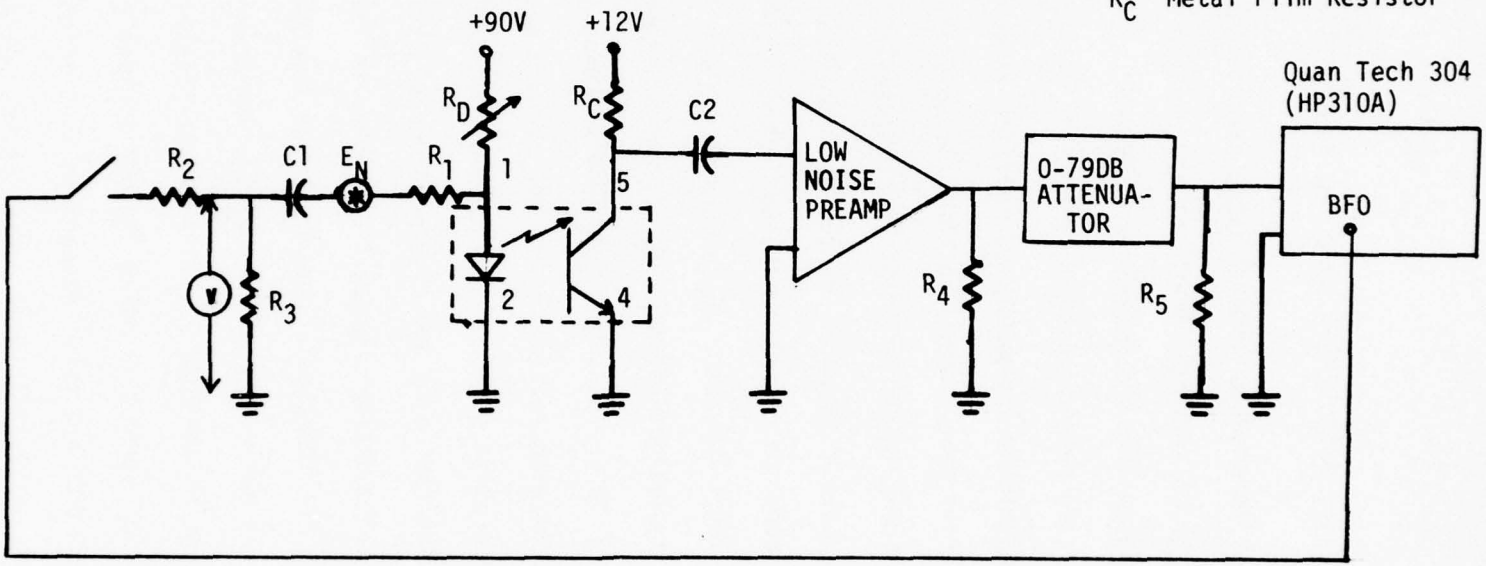
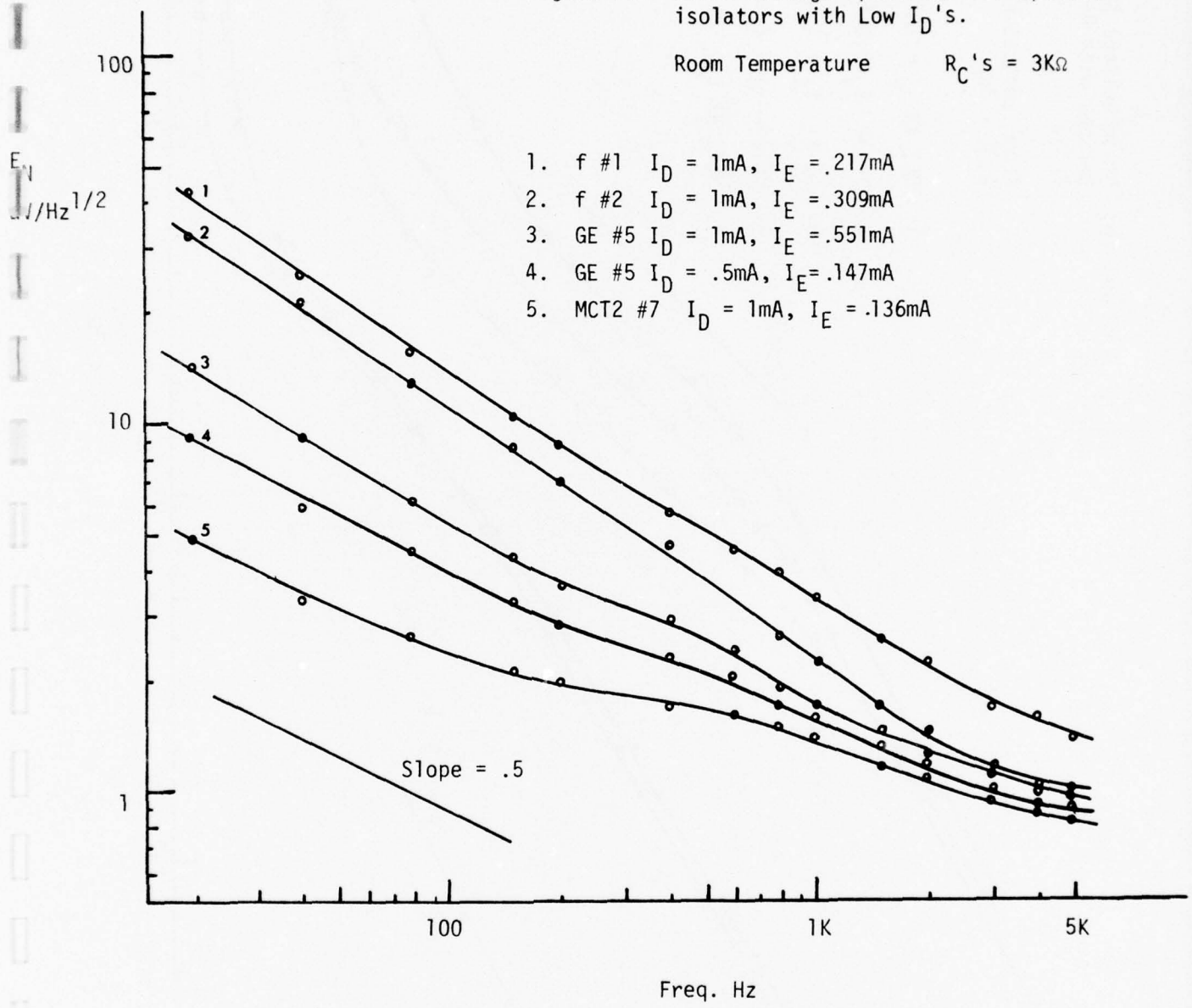


Figure 7A: Noise Voltage Spectrums for Optical-isolators with Low I_D's.

Room Temperature R_C's = 3KΩ

1. f #1 I_D = 1mA, I_E = .217mA
2. f #2 I_D = 1mA, I_E = .309mA
3. GE #5 I_D = 1mA, I_E = .551mA
4. GE #5 I_D = .5mA, I_E = .147mA
5. MCT2 #7 I_D = 1mA, I_E = .136mA



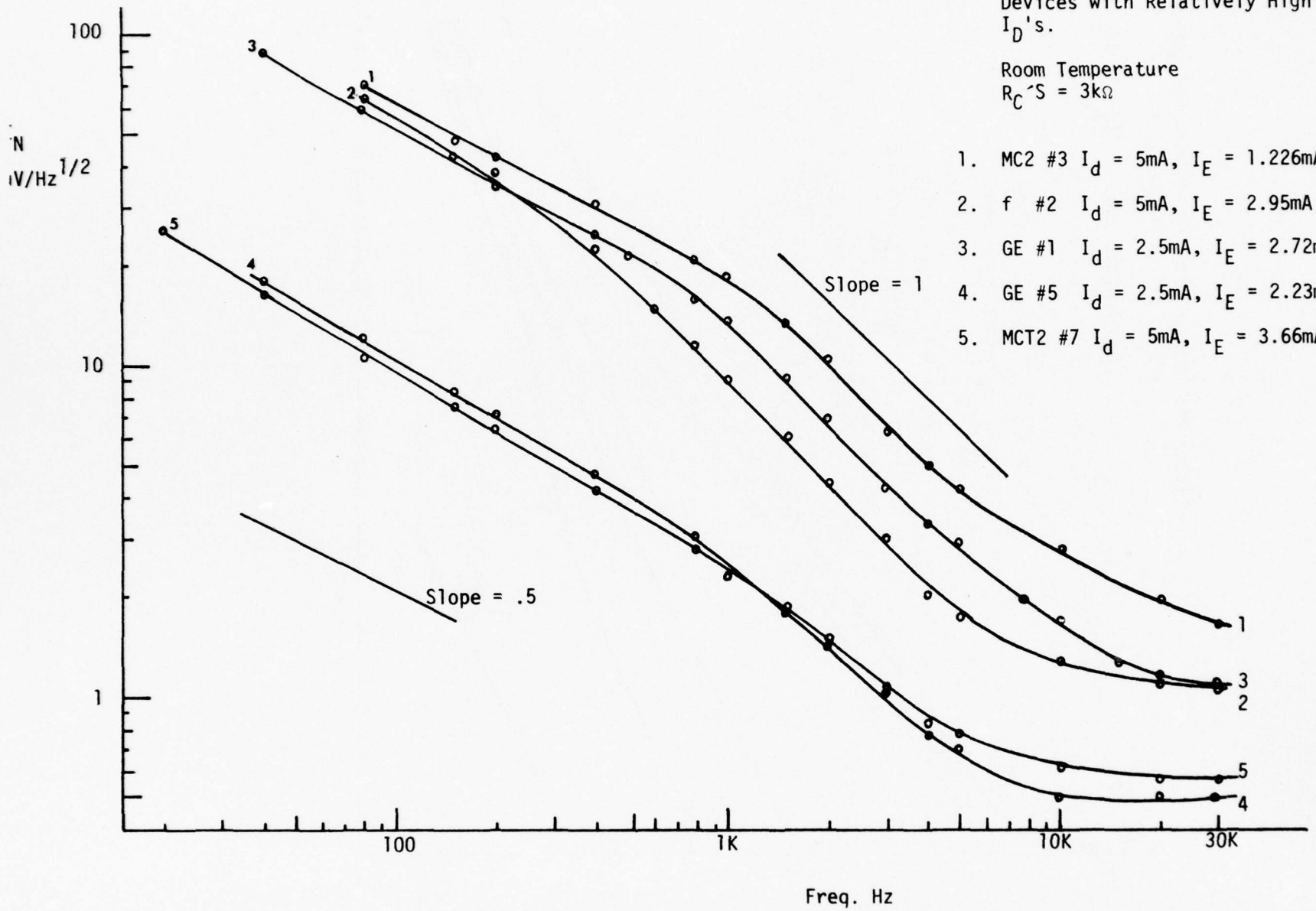


Figure 7B: Noise Voltage Spectrums for Devices with Relatively High I_D's.

Room Temperature
R_C'S = 3kΩ

1. MC2 #3 I_d = 5mA, I_E = 1.226mA
2. f #2 I_d = 5mA, I_E = 2.95mA
3. GE #1 I_d = 2.5mA, I_E = 2.72mA
4. GE #5 I_d = 2.5mA, I_E = 2.23mA
5. MCT2 #7 I_d = 5mA, I_E = 3.66mA

The break frequencies f_B in figure 7B separate the spectrums in the low frequency into two parts. For frequencies higher than the break frequencies, the spectrums have slopes approximately equal to unity corresponding to the form of power spectrum $f^{-\alpha}$ with α equal to 2. For the frequencies lower than the break frequencies, the spectrums have slopes close to one-half corresponding to the power spectrum $f^{-\alpha}$ with $f^{-\alpha}$ close to unity. The equivalent noise power spectrums for figure 7B, in the low frequency region, can be expressed as

$$\overline{E_N^2(f)} = K_4 f^{-\alpha_1} \quad , \quad \alpha_1 \doteq 1 \text{ for } f < f_B \tag{8}$$

$$\overline{E_N^2(f)} = K_5 f^{-\alpha_2} \quad , \quad \alpha_2 = 2 \text{ for } f_B < f < f_5$$

where K_4 and K_5 are constants and f_5 is the frequency where shot noise begins to dominate. K_4 and K_5 are functions of I_D and some other factors that will be examined further in future work.

Figure 8 shows the dependence of equivalent input noise spectrums on I_D. The spectrums can be described with equation (8) and (9). The break frequencies are around 600 H_z.

Both figure 9 and figure 10A show the dependence of noise voltage spectrums on I_D. Again all the spectrums can be approximated with equation (8) and equation (9). For frequencies higher than the break frequency, the curve resembles the form of burst noise, but it will take the form of excess noise for frequencies lower than the break frequency.

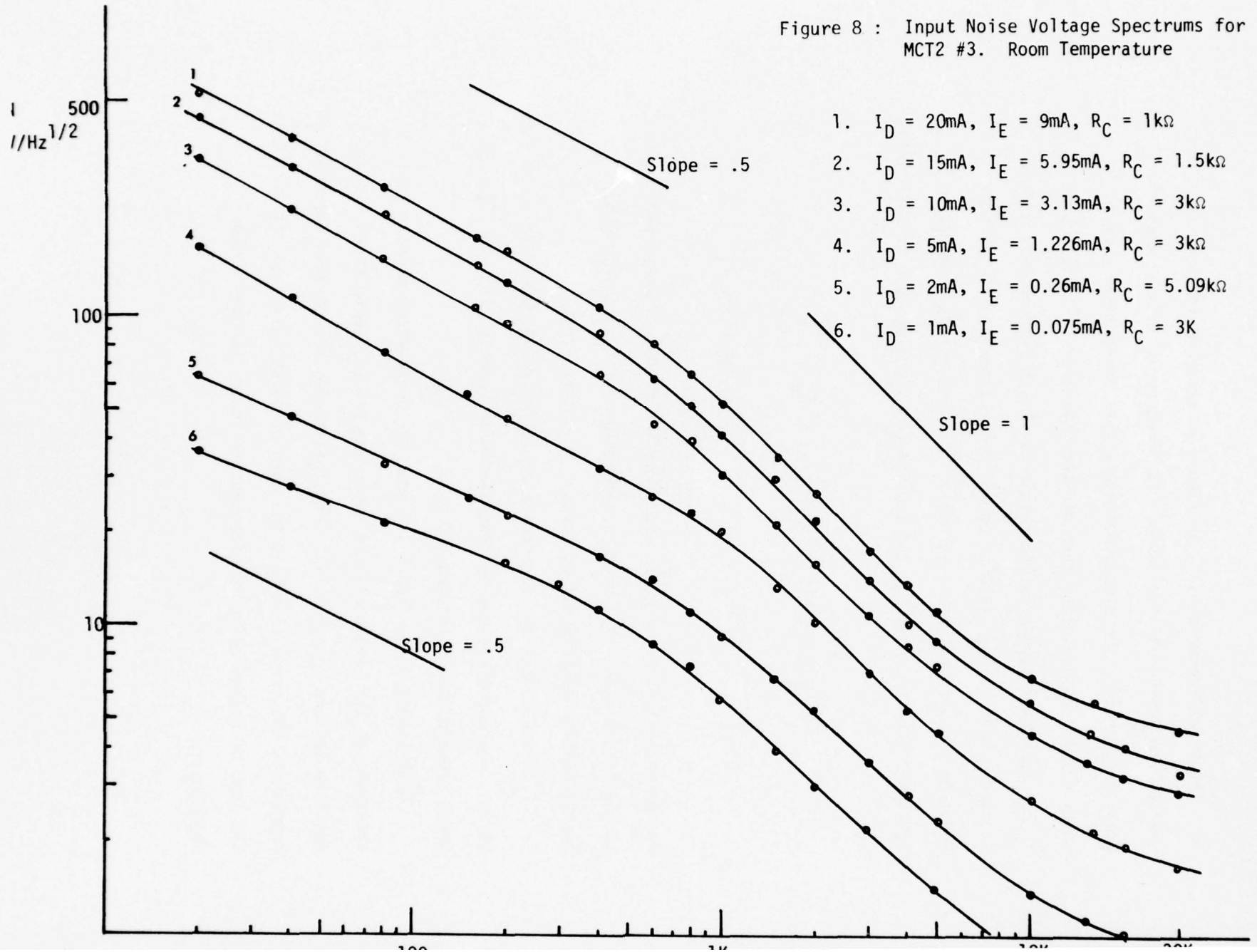
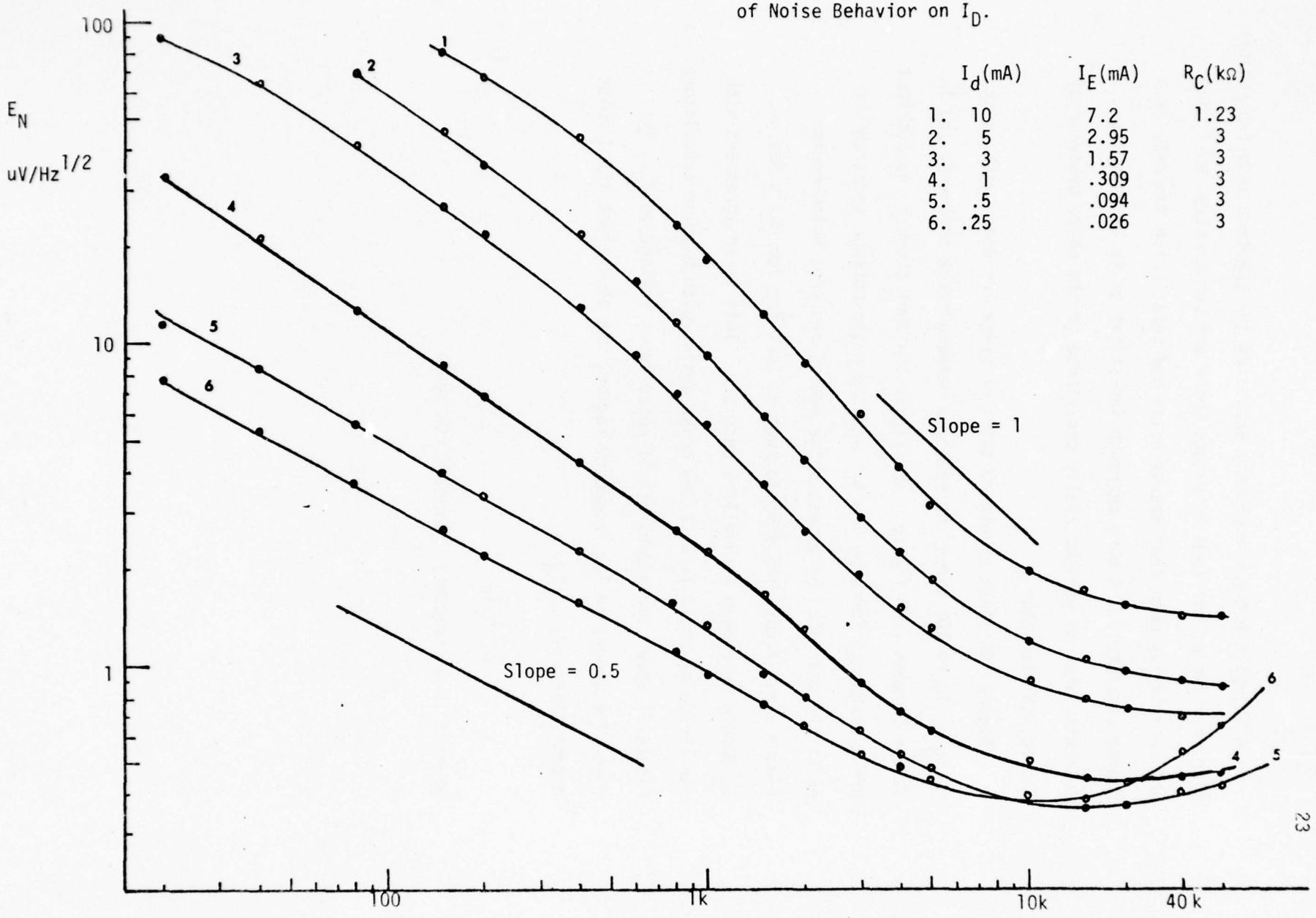


Figure 8 : Input Noise Voltage Spectrums for MCT2 #3. Room Temperature

1. I_D = 20mA, I_E = 9mA, R_C = 1kΩ
2. I_D = 15mA, I_E = 5.95mA, R_C = 1.5kΩ
3. I_D = 10mA, I_E = 3.13mA, R_C = 3kΩ
4. I_D = 5mA, I_E = 1.226mA, R_C = 3kΩ
5. I_D = 2mA, I_E = 0.26mA, R_C = 5.09kΩ
6. I_D = 1mA, I_E = 0.075mA, R_C = 3K

Figure 9: Noise Voltage Spectrums of f #2 Showing Dependence of Noise Behavior on I_D.



	I_d(mA)	I_E(mA)	R_C(kΩ)
1.	10	7.2	1.23
2.	5	2.95	3
3.	3	1.57	3
4.	1	.309	3
5.	.5	.094	3
6.	.25	.026	3

Although the break frequency separates the spectrum into two regions characterized by the form of excess noise and burst noise, this does not necessarily mean that excess noise and burst noise dominate each region separately. A more thorough investigation is necessary to determine what mechanisms really contribute to the noise behavior of the optical-isolator.

Figure 10A shows a uniform shift of break frequency with respect to I_D. Figure 10B shows the relation between break frequency and I_D. It can be seen from figure 9 and figure 10A that there is no distinct break frequency for very low I_D, and the noise voltage spectrum can be simply described by excess noise region and shot noise region. Figure 9 and figure 10A seem to suggest that for low noise design, I_D should be chosen as small as possible. This is in agreement with the choice of small I_C in a low noise design with bipolar transistors. Figure 11 shows the dependence of noise input voltage on I_D. For fixed frequency, in low frequency region, the equivalent input noise depends linearly on I_D.

$$E_N = K I_D \tag{10}$$

where K is a frequency dependent constant.

Figure 10A: Noise Voltage Spectrums
Device IL-5
Room Temperature

	I_D(mA)	I_E(mA)	R_C(KΩ)
1.	10	7.62	1.22
2.	5	2.81	3
3.	2	.667	3
4.	1	.195	3
5.	.5	.052	3
6.	.25	.012	3

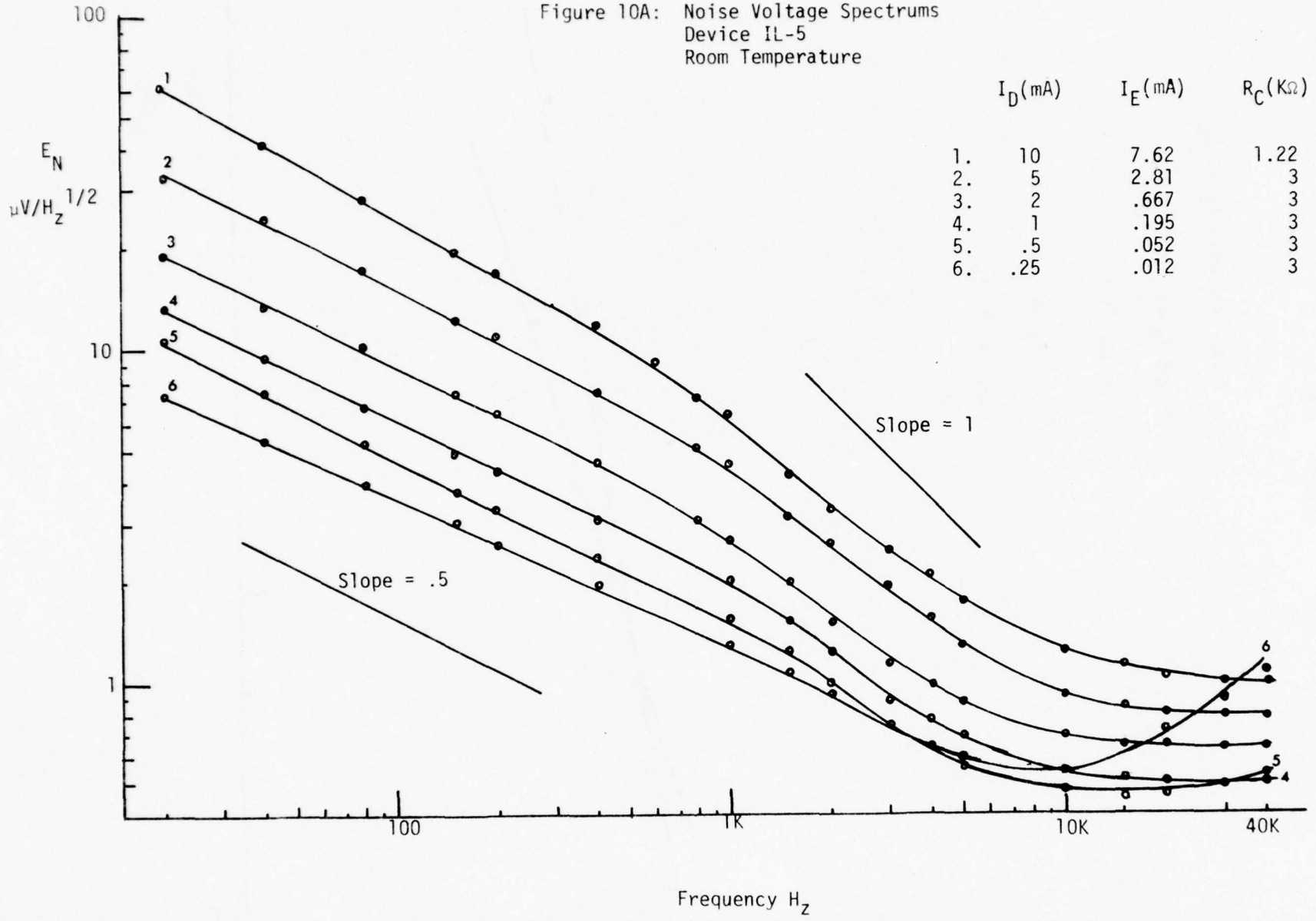


Figure 10B

Break Frequency f_B vs I_E

and f_B vs I_D

Deivce IL-5

1. f_B vs I_D
2. f_B vs I_E

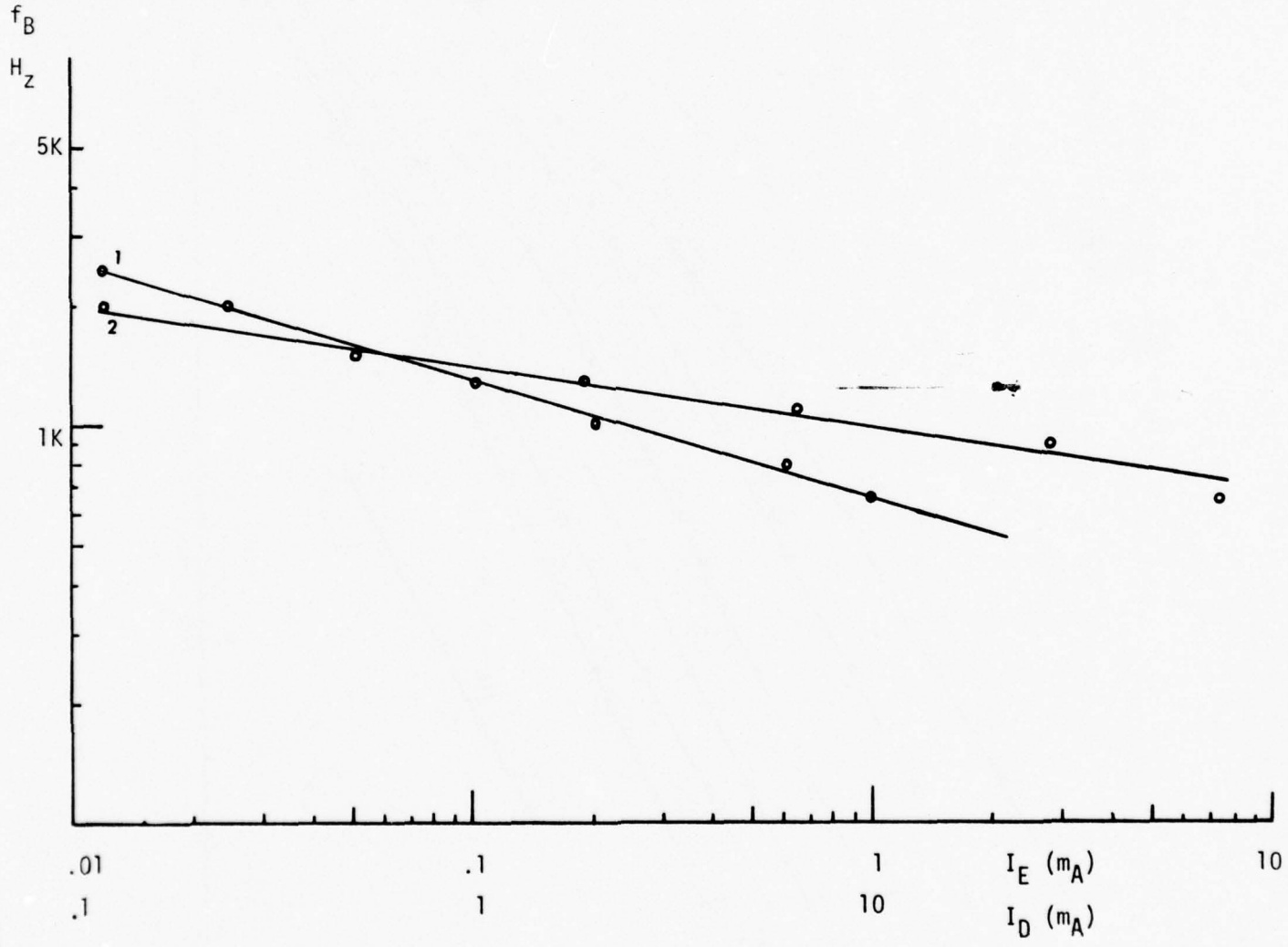
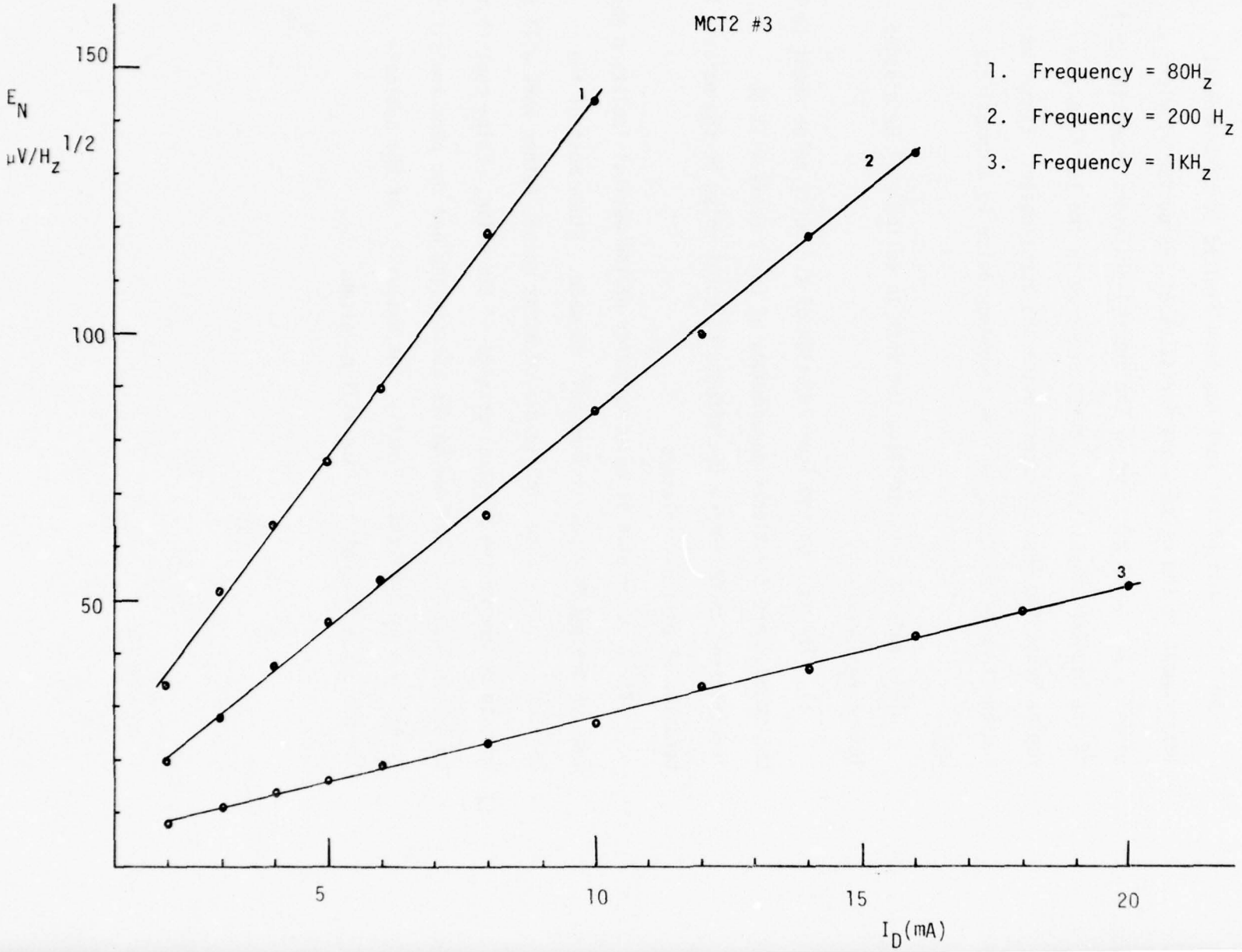


Figure 11

E_N vs I_D

R_C = 1KΩ

MCT2 #3



1. Frequency = 80H_z
2. Frequency = 200 H_z
3. Frequency = 1KH_z

VII. CONCLUSIONS

So far, most of the work has been limited to experimental measurement on the noise characteristics of the optical-isolators. In general, the noise behavior of the optical-isolators resembles that of the bipolar transistors. Noise spectrum in the low frequency region takes the form of excess noise and burst noise. Excess noise and burst noise dominate the low frequency noise in a complicate way.

This work is not complete, the work to follow will be divided into three parts:

(1) The work on the investigation of the burst noise needs to be continued, more functional dependences of burst noise will be investigated to determine the effects of burst noise on the noise behavior of optical-isolators.

(2) A comparison of noise behavior of the optical-isolators and that of the bipolar transistors will be made. Since most of the optical-isolators show high levels of burst noise, futher work will be done to determine the physical origins of the noise. Noise contribution to the optical-isolator due to the LED biasing and the phototransistor itself will be analyzed. Finally, the evaluation of the optical-isolator as a low noise device will be given.

(3) An analytical form for the noise model of optical-isolators will be derived such that the noise characteristic of the device can be expressed in terms of measurable parameters.

Appendix 1

DERIVATION OF EQUIVALENT BURST NOISE CURRENT AMPLITUDE

Figure A1 is used in the derivation of equivalent burst noise current amplitude.

Assuming the burst noise current through LED is I_{BN}, burst noise voltage at the output of the device is

$$M1 = I_{BN} \cdot G \ , \tag{A1}$$

where G is the transresistance from LED to the output.

With a sinewave input from A and G with RMS voltage V, a current with peak to peak value I_S is passed through LED causing a peak to peak sinewave voltage

$$M2 = I_S \cdot G = 2.828\ V \frac{1}{R_1+R_{2//}(R_4+\gamma d)} \cdot \frac{R_2}{(R_4+\gamma d)+R_2} \cdot G \tag{A2}$$

where R_1 = 10.21KΩ, R_2 = 97Ω, R_4 = 1.9KΩ, $\gamma d \ll R_4$.
Equation (A2) can be simplified, with $\gamma d \ll R_4$, as

$$M_2 = 2.828\ V \frac{R_2}{(R_1+R_2)(R_2+R_4)} \cdot G \quad . \tag{A3}$$

Solve equation (A1) and equation (A3) for I_{BN},

$$I_{BN} = 2.828\ V \frac{(\frac{M1}{M2})\ R_2}{(R_1+R_2)(R_2+R_4)} \quad . \tag{A4}$$

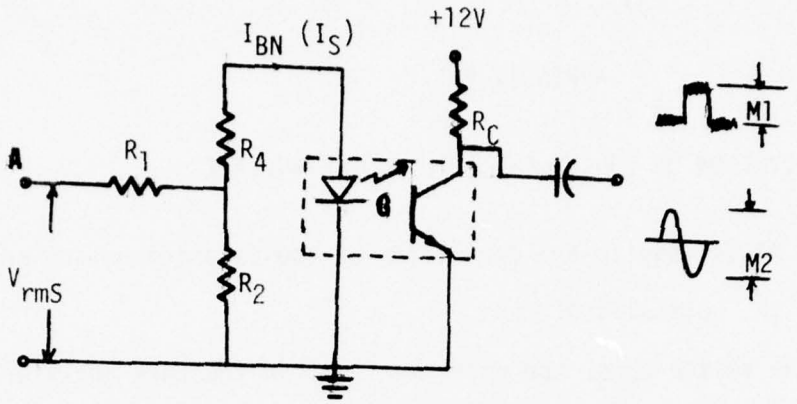


Figure A1

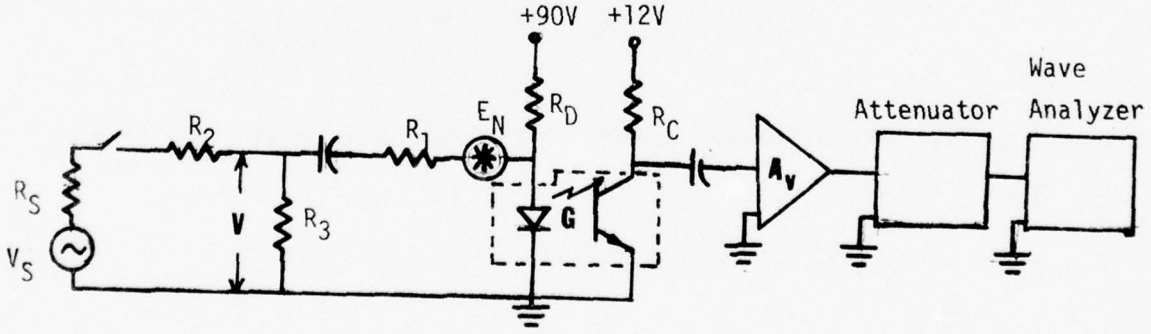


Figure A2

APPENDIX 2

DERIVATION OF EQUIVALENT INPUT NOISE VOLTAGE

Figure A2 is used in the derivation of equivalent input noise voltage for the optical-isolator.

With the switch open, the noise measured on the wave analyzer with noise bandwidth Δf is M1,

$$(M1)^2 = \left[E_N \cdot \frac{\gamma d // R_D}{(R_1+R_3)+ \gamma d // R_D} \cdot G \cdot A_v\right]^2 \Delta f \qquad (A5)$$

where E_N is the equivalent noise input voltage to the system, γd is incremental resistance of LED, Δf is the noise bandwidth of the wave analyzer.

Since $\gamma d << R_D$, equation (A5) can be simplified as

$$(M1)^2 = \left[E_N \frac{\gamma d}{(R_1+R_3)+\gamma d} \cdot G \cdot A_v\right]^2 \Delta f \qquad (A6)$$

$$= \left[K E_N \cdot G \cdot A_\gamma\right]^2 \Delta f \ , \quad K = \frac{\gamma d}{(R_1+R_3)+\gamma d} \ .$$

With the switch on, the RMS voltage measured on wave analyzer is M2,

$$M2 = \left[K^2 (E_N^2 \Delta f + V^2)\right]^{1/2} \cdot G \cdot A_v \cdot Att \qquad (A7)$$

where $Att = 10^{\frac{-dB}{20}}$

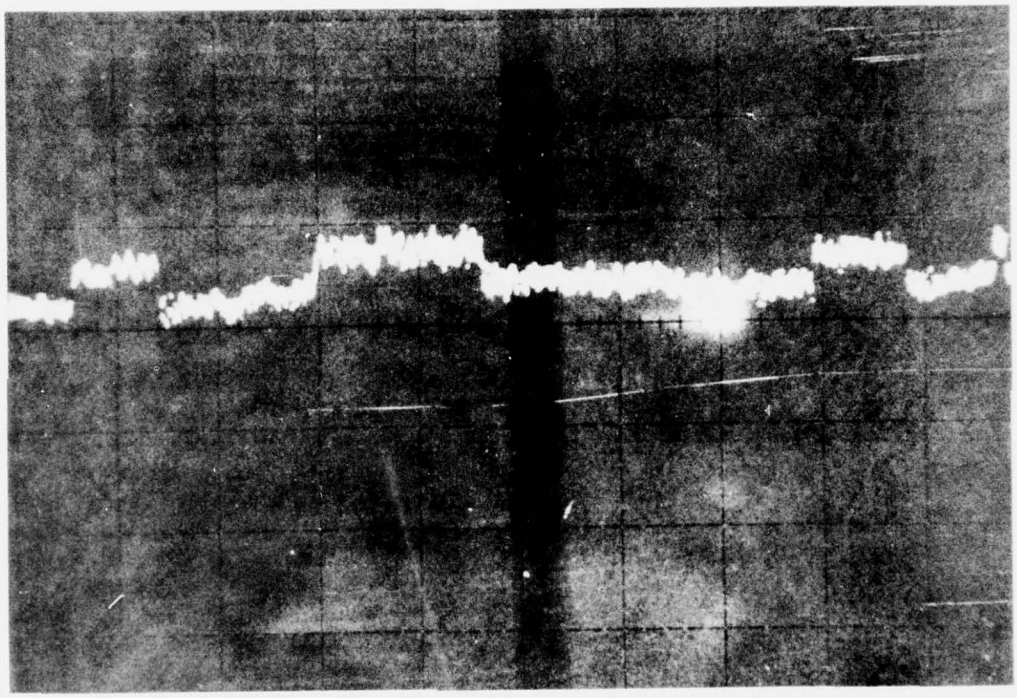
Set M1 = M2 by adjusting the attenuation and solve for E_N,

$$E_N^2 \, \Delta f = V^2 \frac{(Att)^2}{1-(Att)^2} \tag{A8}$$

$$E_N = V \left(\frac{Att^2}{1-Att^2}\right)^{1/2} \cdot \Delta f^{-1/2} \tag{A9}$$

A correction factor 1.13 must be included in equation (A9), thus

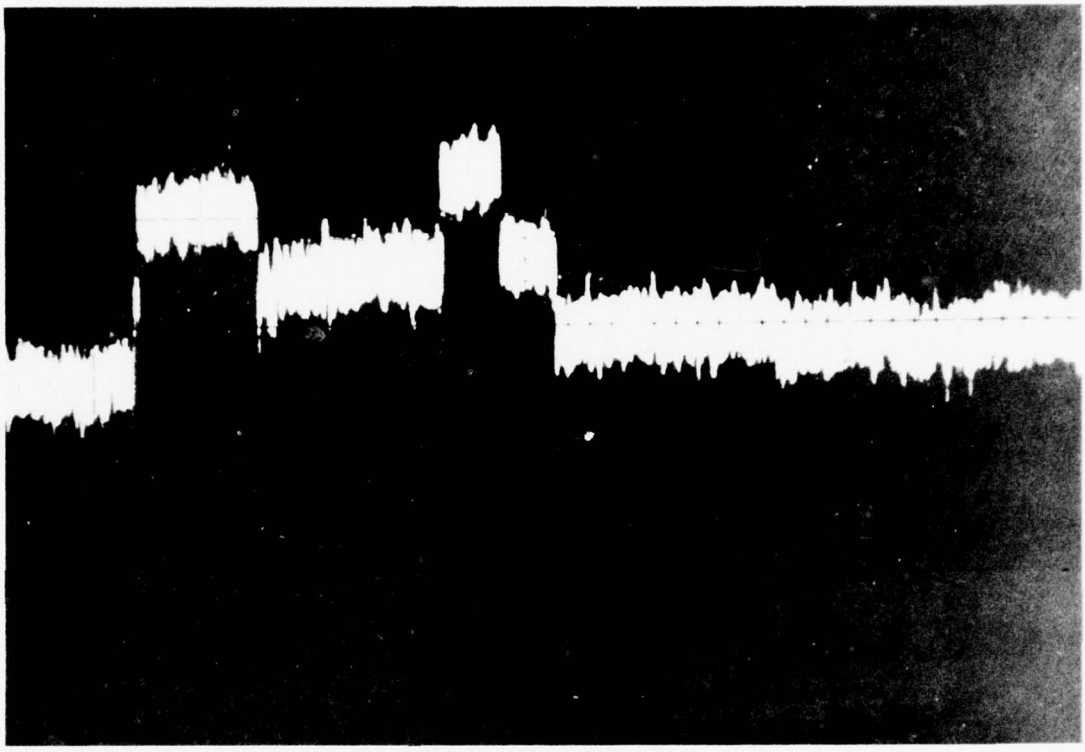
$$E_N = 1.13V \left(\frac{Att^2}{1 - Att^2}\right)^{1/2} \cdot \Delta f^{-1/2} \tag{A10}$$



Burst noise found in MCT2

Horizontal 2 mS/D

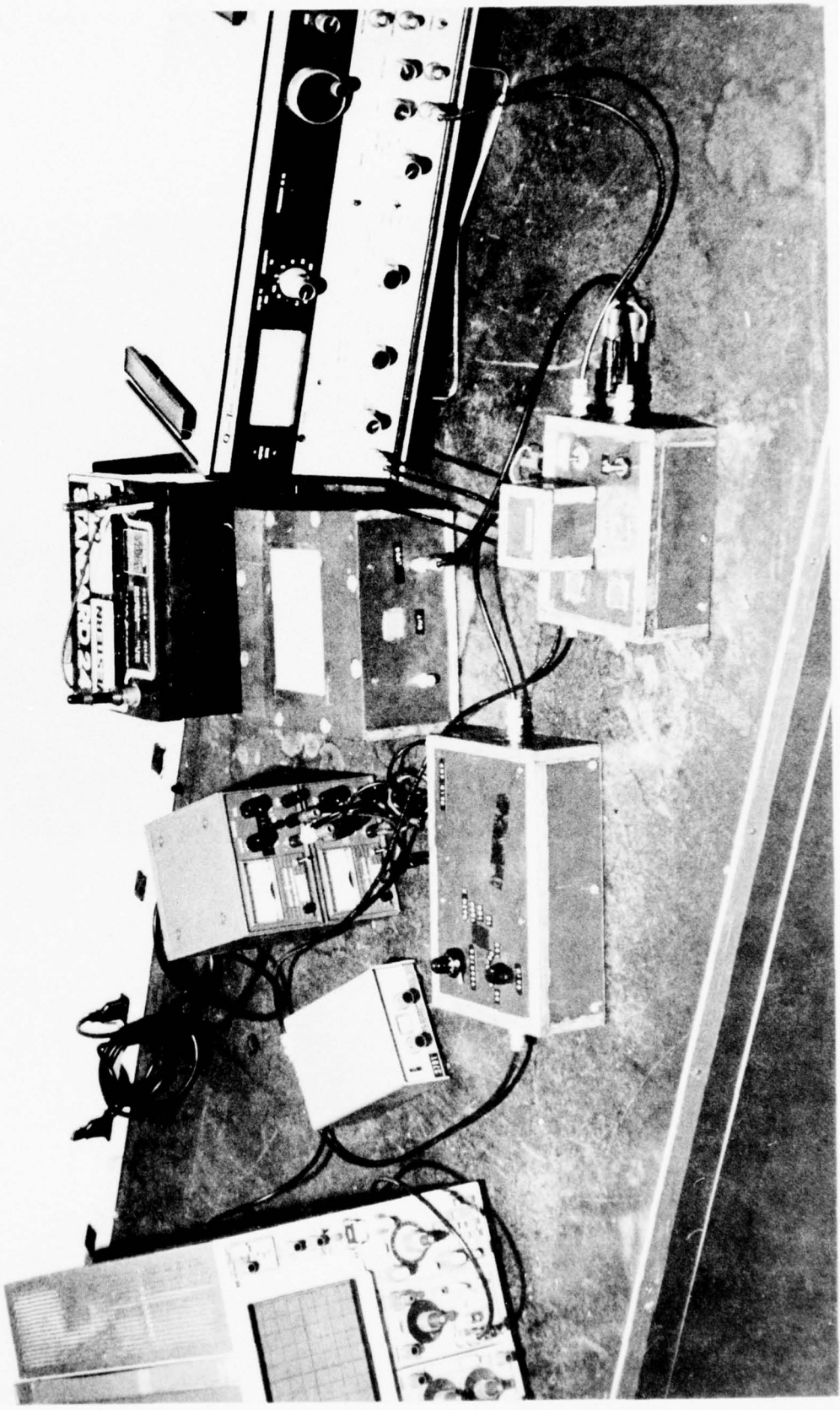
Vertical 1 mV/D



Burst noise found in Motorola 4N26.

Horizontal 10 ms/D

Vertical 2 mV/D



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Part 7

AUTOMATED CONDUCTOR ROUTING

Prepared for

U. S. Army Missile Command
Redstone Arsenal, Alabama

Under

Contract DAAH01-76C-0328

by

Electrical Engineering Department
Auburn University
Auburn, Alabama

Prepared by: Stanley S. Kawka

Reviewed by: B. D. Carroll
Co-Project Leader

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I. PROBLEM STATEMENT

The aim of this project is to develop a computer program that will automatically route the interconnections present in a hybrid circuit. The hybrid board routing problem is assumed to be equivalent to printed circuit board routing.

The basic problem is to connect pairs of points with a path that avoids previously laid paths. With the hundred or more connections that must be made for each circuit, the problem lends itself to solution by computer. The algorithm used in solving this problem must meet the two following requirements:

- The algorithm should determine the shortest path that meets all constraints imposed by the designer with the minimum likelihood of preventing future connections.
- The algorithm must have reasonable requirements of computer memory and execution time.

II. ALGORITHM DESCRIPTION

The algorithm being developed to meet those requirements will now be described. The router will presently work on boards with up to eight layers with each board measuring up to 15" x 15" assuming 5 mils between conductor paths. The approach used is to treat the interconnection of layers by means ov vias (or feedthroughs). A coded array that is stored in memory, records all information about the state of the board. The actual routing algorithm consists of a series of iterative steps that use an extension of Lee's Algorithm and that involve decisions on the basis of the state of this array. Routing terminates where all paths have been completed or when all paths have been exhausted.

The CELMAP array (C-array) is set up in memory as shown in Figure 1. Each array position or cell occupies a full word of memory (32 bits), with each of these words further divided into four fields (bytes). The fields, described in Figure 2, are now defined:

- The sequence or S-field is used to record the marking sequence. To conserve memory space a 1-2-3 marking sequence is used with a Ø being used to signify an unmarked cell.
- The availability or A-field is used to record whether a cell is occupied or unoccupied on each later. For each layer, a value of 1 denotes an unoccupied cell and 0 an occupied one.

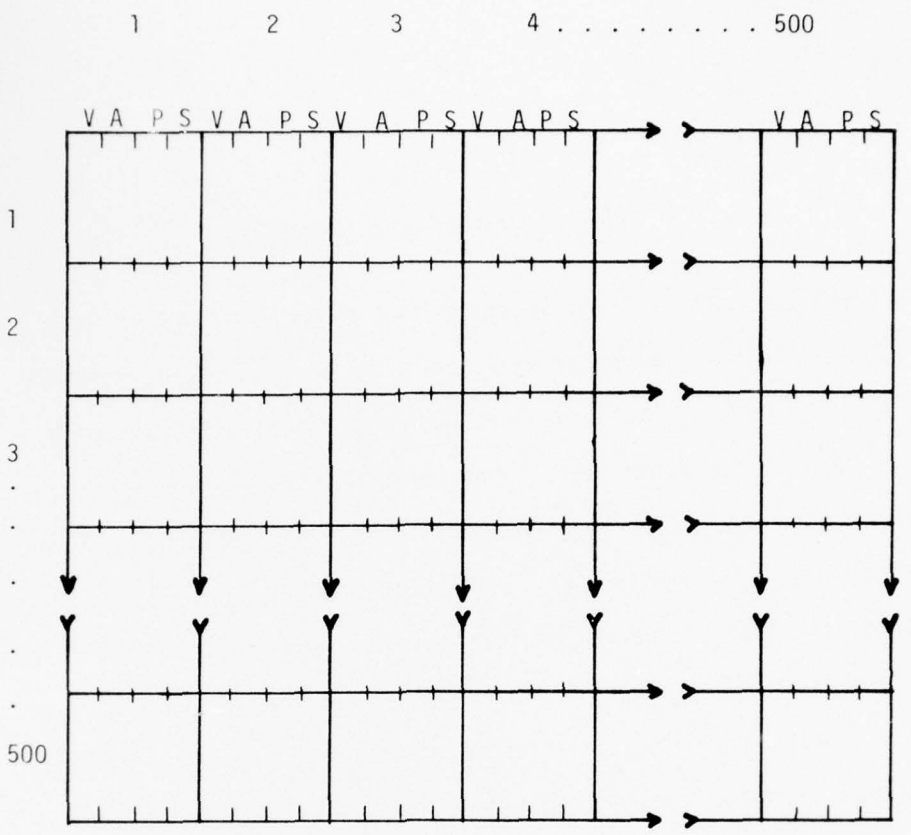


Figure 1. Description of Celman Array

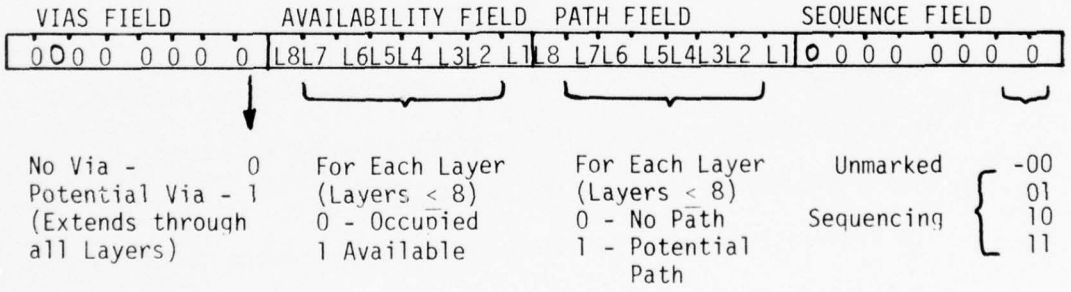


Figure 2. Description of a Cell

·The path or P-field is used to record the unoccupied layers in the availability field on which a potential connection path to a marked cell has been discovered. For each layer, a value of 1 denotes a potential connection path whereas 0 indicates no path.

·The vias or V-field records potential via cells. A value of 1 denotes a potential via. ($V = 1$ if $\prod_{i=1}^{8} A_i = 1$).

Now that one is familiar with the array and with the information stored in it, the routing algorithm will be presented step by step.

Step 1) Retrieve the path field from the starting cell.

Step 2) Determine the layers on which a connection path may leave the starting cell. If the vias field for the starting cell is 0, then the path field identifies the layers on which a connection path may leave the starting cell; otherwise, the starting cell is a potential via, and a path may leave on any layer.

Step 3) Determine the neighboring cells to the starting cell using Lee's Algorithm.

Step 4) For each neighboring cell, determine if the cell is unmarked on a previous cycle. ($S_2S_1 = 00$)

Step 5) For each neighboring cell that is unmarked on a previous cycle, test for a possible path from the starting cell to the neighboring cell. A path exists if for any of the layers on which a connection path may leave the

starting cell as determined in Step 2 there exists a 1 in the corresponding layer but in the availability field of the neighboring cell.

Step 6) Record any paths to the neighboring cells that are found in Step 5 by:

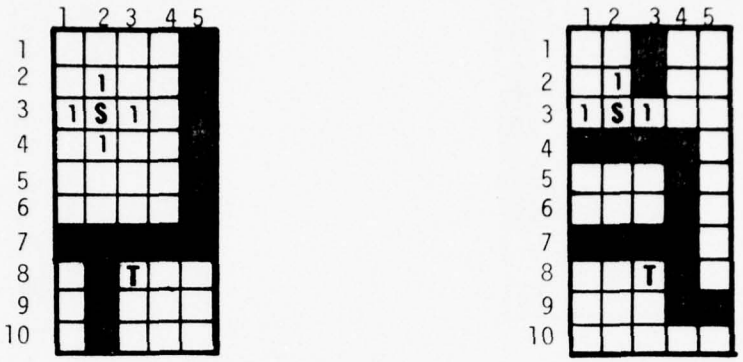
(1) Marking the S-field of the neighboring cell with the present value.

(2) Recording the layers on which the path exists by storing a 1 in its corresponding layer positions in the path field (For $i = 1,\ldots,8$; $P_{i_N} = P_{i_S} \cap A_{i_N}$)

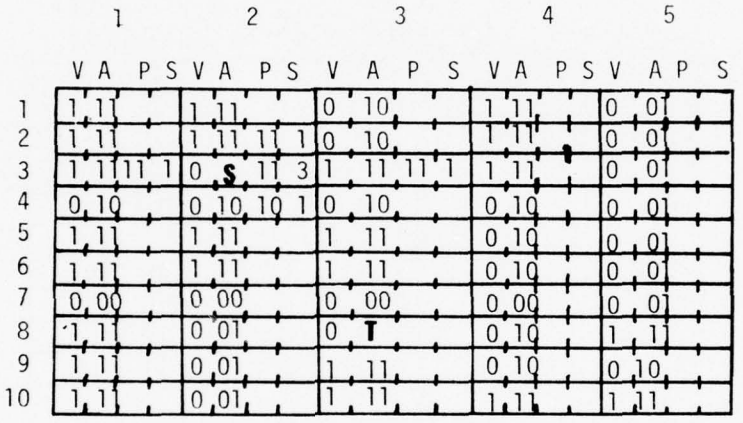
Step 7) Make each of the neighboring cells that are in the path a new starting cell and repeat.

Figures 3 and 4 illustrate the application of the steps just mentioned. Retracing the path upon completion (reaching the target cell) is easy providing the following two conditions are sufficient:

- The S-field mark on the next potential cell on the path must equal the current value.
- Either the V-field of the next potential cell on the path must be a 1 or the P-field must contain a 1 in a position that corresponds to at least one of the layers on which a path may reside on the last determined cell on the path. The layers on which a path may reside are determined by anding the P-field of all cells along the path from the last cell used as a via.

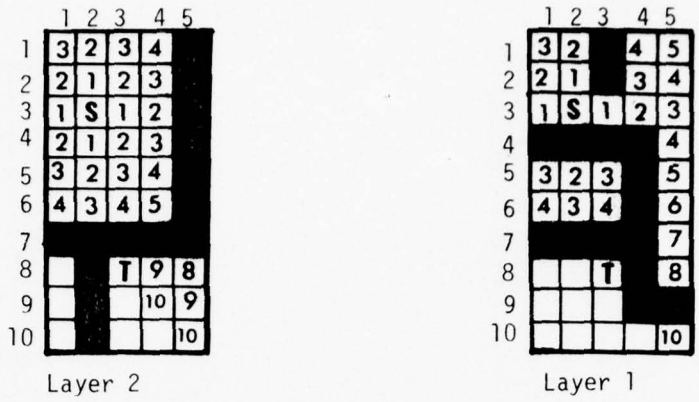


(a)



(b)

Figure 3. (a) Simple Two-Layer Board With Several Paths Already Completed and Another to be Routed From S to T. (b) C-Array for the Two Layers is Shown After Completion of 1 Cycle.



(a)

(b)

Figure 4. After 10 Cycles The Path From S To T Is Completed .

Figure 5. C-Array Has Now Been Updated To Include The Path Between S And T. The Algorithm Can Now Be Repeated With The Next Pair Of Points To Be Connected.

Once a path route is chosen, the C-array is updated to show the new path by:

(1) Removing the layer bit of the path in the A-field and setting the via bit to 0 for all cells along the path.

(2) Setting the A-field to 0 for any cell used as a via along the path.

(3) Resetting the P-field and S-field to 0 throughout the entire array.

The updated array for our example is given in Figure 5.

III. DEVELOPMENT STATUS

At the present time coding of this routing algorithm has been completed (See accompaning flowchart, Figure 6) and testing is underway. This leaves usable input and output connections to the algorithm to be developed. Once this is completed the router will be usable. Further programming, however, will continue to make the router more efficient. Techniques of ordering the connections, framing part of the board to the path, and interactive control over the routing process are planned.

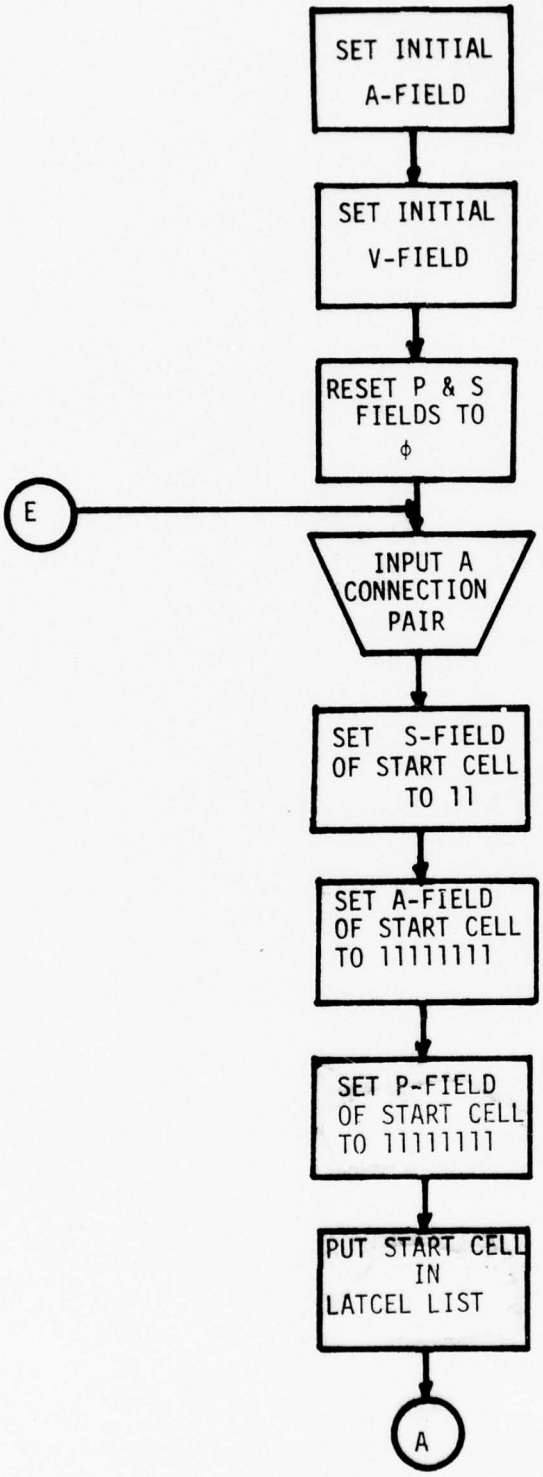
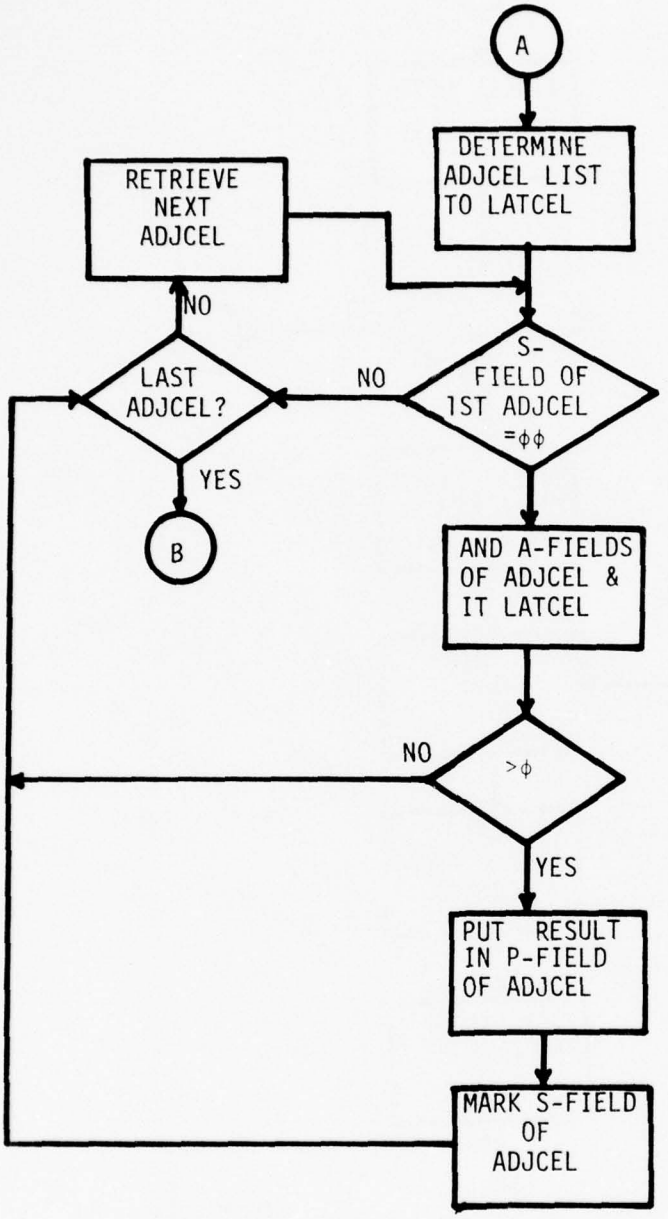
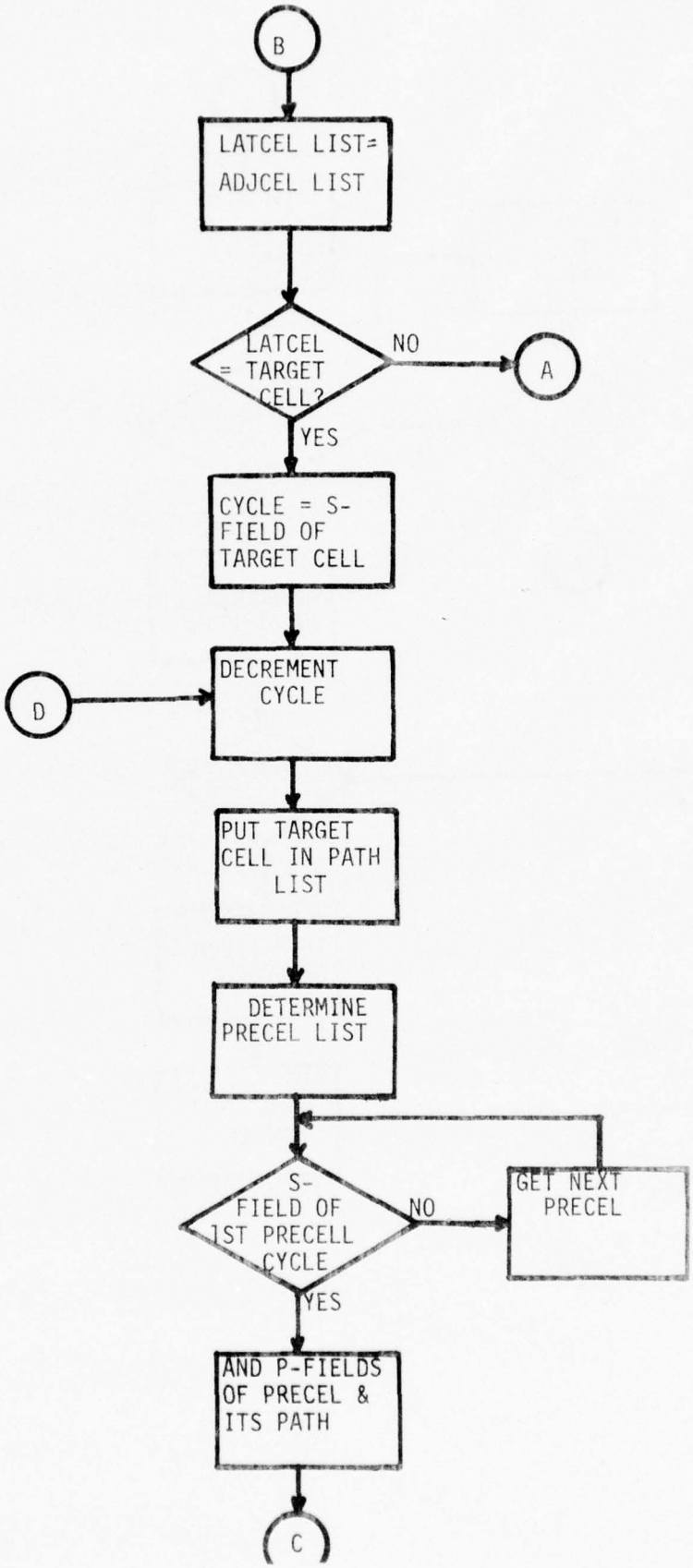
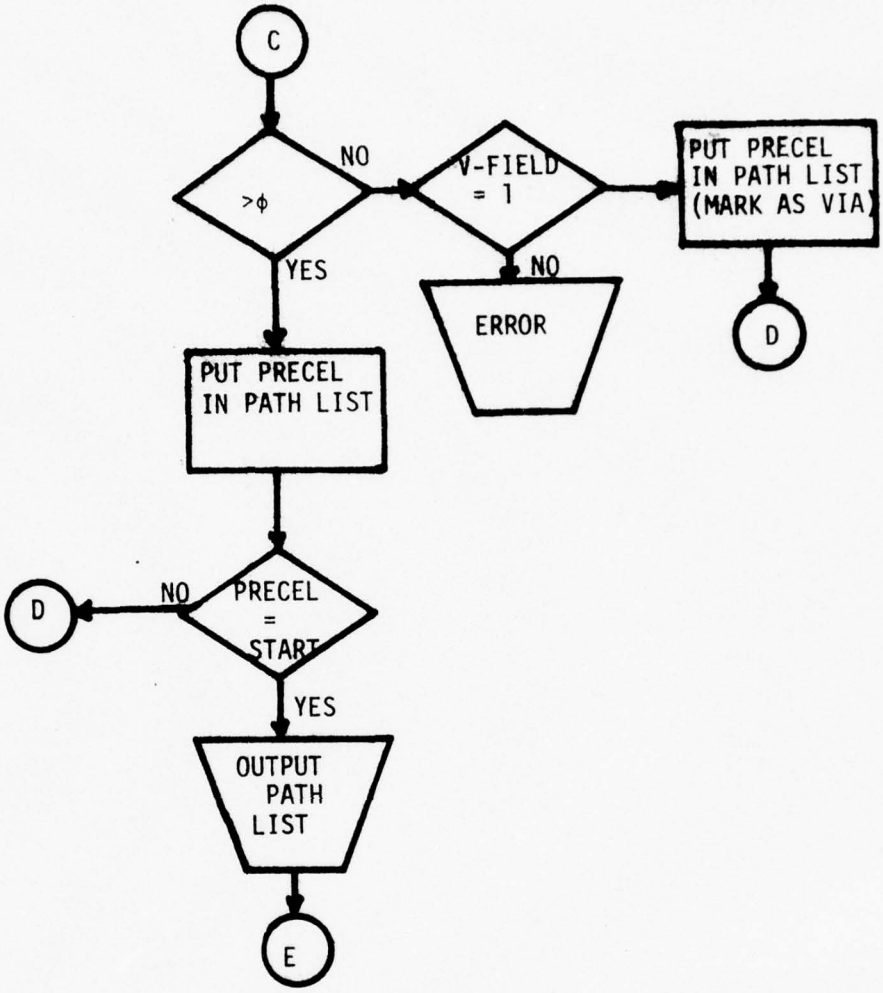


Figure 6. Flowchart Of Routing Algorithm


A
DETERMINE ADJCEL LIST TO LATCEL
RETRIEVE NEXT ADJCEL
NO
S-FIELD OF 1ST ADJCEL =φφ
NO
LAST ADJCEL?
YES
B
AND A-FIELDS OF ADJCEL & IT LATCEL
NO
>φ
YES
PUT RESULT IN P-FIELD OF ADJCEL
MARK S-FIELD OF ADJCEL


B
LATCEL LIST= ADJCEL LIST
LATCEL = TARGET CELL?
NO
A
YES
CYCLE = S-FIELD OF TARGET CELL
D
DECREMENT CYCLE
PUT TARGET CELL IN PATH LIST
DETERMINE PRECEL LIST
S-FIELD OF 1ST PRECELL CYCLE
NO
GET NEXT PRECEL
YES
AND P-FIELDS OF PRECEL & ITS PATH
C


C
>ϕ
NO
V-FIELD = 1
PUT PRECEL IN PATH LIST (MARK AS VIA)
NO
ERROR
D
YES
PUT PRECEL IN PATH LIST
D
NO
PRECEL = START
YES
OUTPUT PATH LIST
E

Part 8

Interactive Schematic Program EAGLE

Prepared for

U. S. Army Missile Command

Redstone Arsenal, Alabama

Under Contract

DAAH01-76-C-0328

by

Gerald R. Kane
Assistant Professor
Electrical Engineering Department
Auburn University
Auburn, Alabama

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Interactive Schematic Program - EAGLE

A graphics input language to be used to provide input to a circuit analysis program as outlined in Part 3 was developed using existing facilities at Auburn University. This program is entitled EAGLE which is an acromym for Electronic Analysis Graphic Language Extension. The program is written in BASIC for a RSTS (DEC) system. Its portability to MICOM is assured if the hardware configurations are compatible. The software upgrading of the MICOM system was recommended early in the project development.

EAGLE is capable of producing a data base that contains both graphical and topological data. These two forms are required for the schematic sketcher and the circuit analysis program respectively. A simple correspondence between these two data types is established by forcing key graphic features to a fixed grid spacing in the display. The size of the grid mesh is fine enough not to distract the user and coarse enough to permit easy sorting and association of graphic and topological inputs. The x, y position of a component is established by the crosslair mechanism of the TEKTRONIX 4000 series graphics terminals. Circuit features are specified by a single character:

N - establish node

W - draw a wire

R - add resistor

L - add inductor

C - add capacitor

Q - add transistor

V - add voltage source

I - add current source

M - request menu for addition schematic
saving schematic
editing existing schematic

A number of standard library transistors are available and may be called by name. Additional transistors may be specified by the user. The program relies on a classification in the library to know about sketching the appropriate NPN, PNP or MOS circuit symbol.

An example of design session is presented to show how the design program is utilized.

Figure 1: Begin design session with a voltage source and a 100 mH choke

Figure 2: Add a previously designed portion of the circuit. Called AMP (the system appends an .CKT extension. The file AMP.CKT may be handled as an ASCII file by any system program.)

Figure 3: The single transistor stage is added to the figure.

Figure 4: A 1μF emitter bypass capacitor is added.

Figure 5: The biasing circuit is to be modified (the wire pointer up from the base of Q1.). The program recognizes a number of standard transistors such as 2n2222 as NPN or 2N2907 as PNP.

Figure 6: R4 is added and connected to the lower supply (V_{cc}).

Figure 7: A menu request for the edit mode is shown.

Figure 8: The circuit is drawn one component at a time and the user decides whether to retain the component in his circuit. The 100 mH choke is deleted in this example.

Figure 9: The circuit is shown without the input inductor.

Figure 10: A 10 μF capacitor is added as CIN.

Figure 11: The circuit is saved as File AMP.CKT.

Figure 12: The drawing is reproduced same menu.

The data base AMP.CKT is attached. General Format is

@ X coord. Y coord. .Orientation Type Value

This information is sufficient to produce network information for any circuit analysis program.

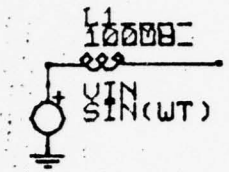

Figure 1: Begin design session with a voltage source and a 100 mH choke

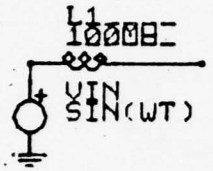

Figure 2: Add a previously designed portion of the circuit. Called AMP (the system appends an .CKT extension. The file AMP.CKT may be handled as an ASCII file by any system program.)

☐ SAVE

☒ APPEND
NAME? AMP

☐ REDRAW

☐ ERASE

☐ EDIT

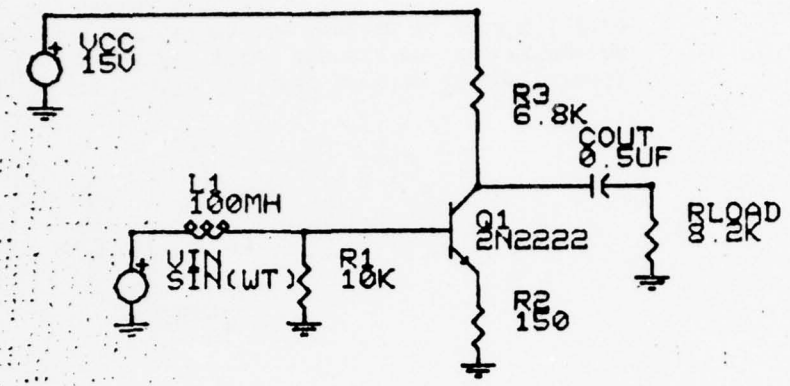

Figure 3: The single transistor stage is added to the figure.

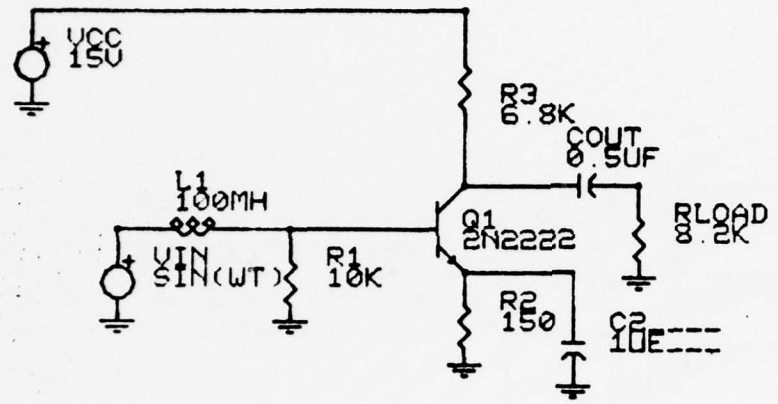

Figure 4: A 1μF emitter bypass capacitor is added.

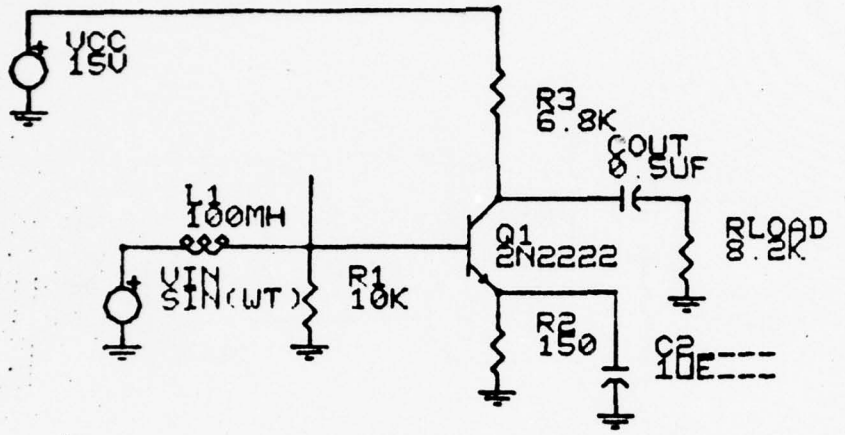

Figure 5: The biasing circuit is to be modified (the wire pointer up from the base of Q1.). The program recognizes a number of standard transistors such as 2N2222 as NPN or 2N2907 as PNP.

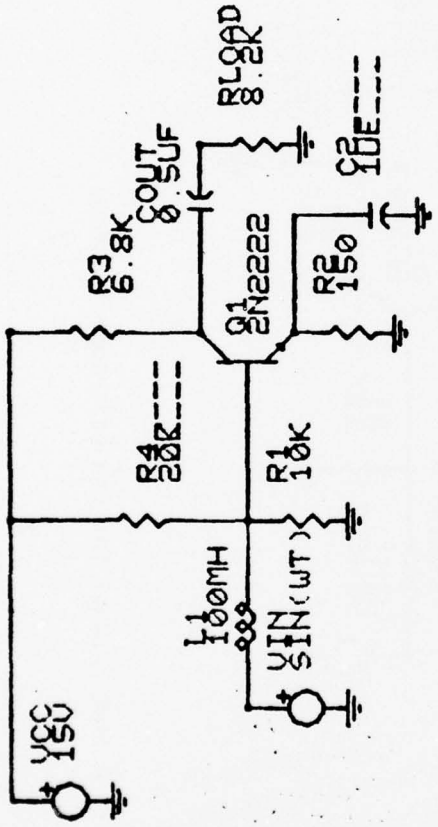

Figure 6: R4 is added and connected to the lower supply (V_{cc}).

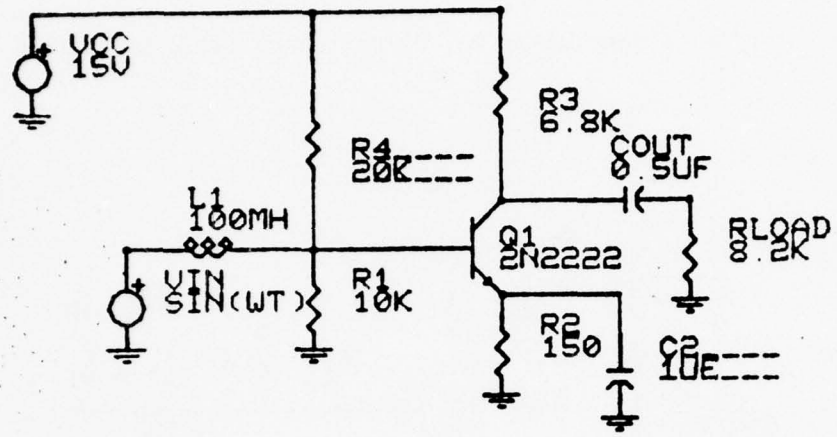

Figure 7: A menu request for the edit mode is shown.

10

☐ SAVE

☐ APPEND

☐ REDRAW

☐ ERASE

X ☐ EDIT

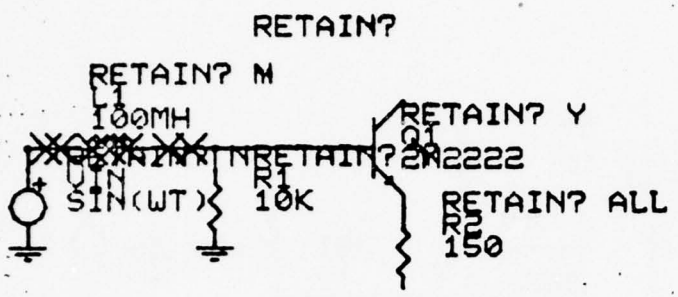

Figure 8: The circuit is drawn one component at a time and the user decides whether to retain the component in his circuit. The 100 mH choke is deleted in this example.

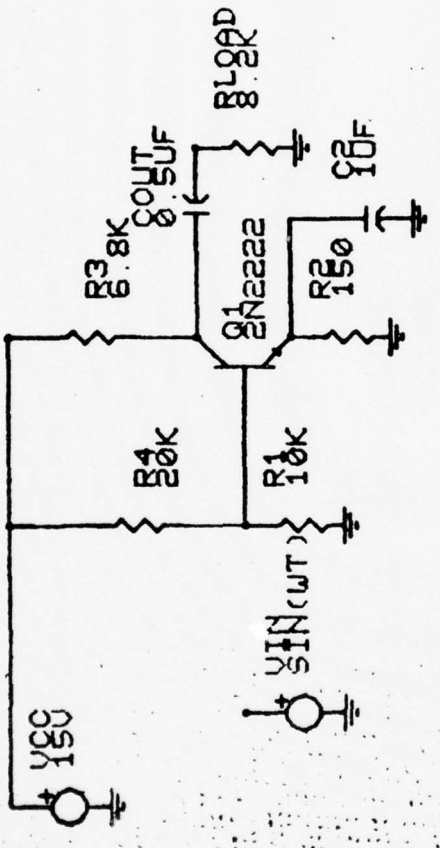

Figure 9: The circuit is shown without the input inductor.

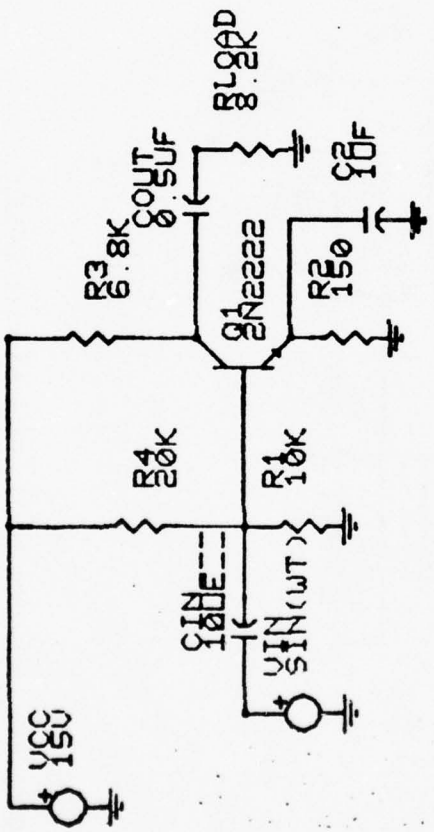

Figure 10: A 10 μF capacitor is added as CIN.

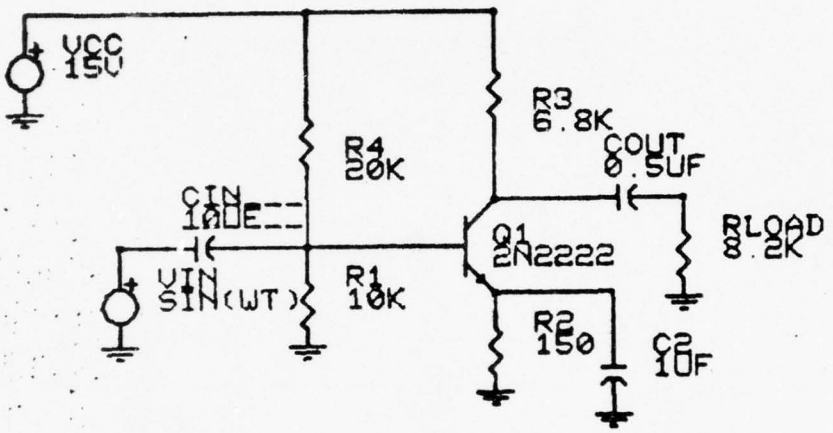

Figure 11: The circuit is saved as File AMP.CKT.

[X] SAVE
NAME? AMP
[ ] APPEND

[ ] REDRAW

[ ] ERASE

[ ] EDIT

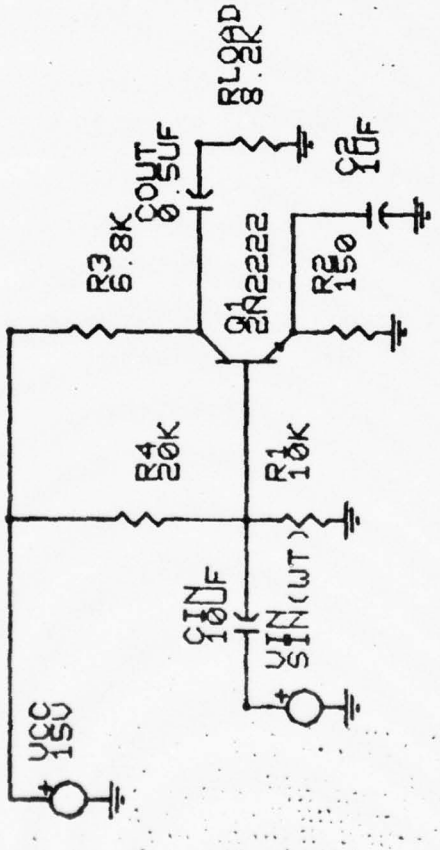

Figure 12: The drawing is reproduced same menu.

AD-A039 503 AUBURN UNIV ALA ENGINEERING EXPERIMENT STATION F/G 9/5
DEVELOPMENT OF TECHNIQUES AND PROCEDURES FOR ADVANCED TOOL DEVE--ETC(U)
1977 B D CARROLL, K B COOK, G R KANE DAAH01-76-C-0328
UNCLASSIFIED AU-EE-AMC-76-0328-1 NL

3 OF 3
AD
A039503

END

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6-77

Recommended Improvements

The EAGLE program is reasonably easy to use once some familiarity with the system is acquired. Extensions and refinements to the program will include

1. A more flexible EDIT mechanism
2. The ability to transfer schematic segments on the screen
3. Self help programs to aid the learning process and assist designer in the programs nuances
4. Careful selection of a specific EAGLE-circuit analysis support program.

With these additions and modifications EAGLE will become an effective tool in the design of electronic circuits.

Reference

Newman, William M. and Sproull, Robert F., Principles of Interactive Computer Graphics, McGraw Hill (1973).

```
EAGLE.BAS                    Created  16-Feb-77  at  10:36

1!!!     EAGLE    VERSION 6A       EDIT 1          16-Feb-77
2!!!
!!!!     PROGRAMMER:  GERALD R. KANE
!!!!
3!!!     AUBURN UNIVERSITY
!!!!     ELECTRICAL ENGINEERING DEPARTMENT
!!!!     AUBURN, ALABAMA
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!!!!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

19!


         !       M O D I F I C A T I O N   H I S T O R Y


99!499
100!


         !       P R O G R A M   D E S C R I P T I O N


300!


         !       I / O   C H A N N E L S


301!     CHANNEL           USED FOR:

400!


         !       V A R I A B L E   D E F I N I T I O N S


401!     VARIABLE          DEFINITION

800!
```

```
EAGLE.BAS                    Created  16-Feb-77  at  10:36

        !       F U N C T I O N S   A N D   S U B R O U T I N E S

801!            !PROGRAMMER DEFINED SUBROUTINES

        !LINE           DESCRIPTION

830!            !PROGRAMMER DEFINED FUNCTIONS

900!

        !       D I M E N S I O N   S T A T E M E N T S

910     DIM S$(100)

920     DIM V%(100)

999!

        !       S T A R T   O F   P R O G R A M

1000    ON ERROR GOTO 19000
        ! ERROR TRAP

1010    Q5$="PNP#2N2907#"

1020    Q6$="NPN#2N2222#"

1030    ! NPN AND PNP TRANSISTOR DIRECTORIES

2000    S$(0%)=NUM$(0%)\GOSUB 9000

2005    E%=0

2010    B$=FNR$
        \X%=(X% AND -16%) OR 8%
        \Y%=(Y% AND -16%) OR 8%
        ! PICUP A COMMAND

2015    B$=CVT$$(B$,32%)

2020    ON INSTR(1%,"GNWRLCQDVIXMS",B$) GOSUB
         3000,3100,3200,3300,3300,3300,3400,3300,
         3300,3300,3500,4000,32766

2030    IF E% THEN GOTO 2000 ELSE GOTO 2010

3000    A$="@"+NUM$(X%)+NUM$(Y%)+".0 G "

3010    X1%=X0%\X0%=X%\Y1%=Y0%\Y0%=Y%

3015    GOSUB 10000
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
3020    I%=VAL(S$(0%))+1%
3030    S$(I%)=A$\S$(0%)=NUM$(I%)\RETURN
3100    A$="@"+NUM$(X%)+NUM$(Y%)
3110    GOTO 3010
3200    A$="@"+NUM$(X0%)+NUM$(Y0%)+"@"+NUM$(X%)+NUM$(Y%)
3210    GOTO 3010
3300    ! INPUT RESISTOR
3310    W1%=X0%-X1%\W2%=Y0%-Y1%
3315    A$="@"+NUM$(X%)+NUM$(Y%)
3320    IF W1%>0 THEN
        IF W2%=0 THEN A$=A$+".0 "
        ELSE IF W2%>0% THEN A$=A$+".7 " ELSE A$=A$+".1 "
3330    IF W1%=0 THEN
        IF W2%>0 THEN A$=A$+".6 " ELSE A$=A$+".2 "
3340    IF W1%<0 THEN
        IF W2%=0 THEN A$=".4 "
        ELSE IF W2%>0% THEN A$=A$+".5 " ELSE A$=A$+".3 "
3350    D$,A$=A$+B$
3360    A$=A$+"_____ _____ "
3370    GOSUB 10000
3380    X1%=X0%\X0%=X%+Q1*48%\Y1%=Y0%\Y0%=Y%-Q2*48%
3390    PRINT FNQ$(2%)+FNP$(Q3%,Q4%)+FNQ$(1%)+" ";\INPUT #1%,T$
3392    PRINT FNQ$(2%)+FNP$(Q3%,Q5%)+FNQ$(1%);\INPUT #1%,K$
3394    A$=D$+T$+" "+K$+" "
3396    GOTO 3020
3400    ! TRANSISTOR
3410    W2%=X0%-X1%
3420    A$="@"+NUM$(X%)+NUM$(Y%)
3430    IF W2%>0% THEN A$=A$+".0 " ELSE A$=A$+".4 "
3440    D$,A$=A$+B$
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
3450    A$=A$+"_____ _______ "

3460    GOSUB 10000

3470    X1%=X0%\X0%=X%+32%*Q1\Y1%=Y0%\Y0%=Y%-32%

3480    GOTO 3390

3500    ! DELETE

3510    I%=VAL(S$(0%))

3520    A$=S$(I%)

3530    IF I%=0% THEN RETURN

3540    S$(0%)=NUM$(I%-1%)

3550    IF LEFT(A$,1%)<>"@" THEN GOTO 3500
        ! DELETE NON GRAPHIC CARD

3560    B$=CVT$$(RIGHT(A$,2%),1%+4%+8%+16%+32%)
        ! DROP THE @ SIGN

3570    R%=INSTR(1%,B$," ")
        \X%=VAL(LEFT(B$,R%))
        \B$=CVT$$(RIGHT(B$,R%),8%)

3580    R%=INSTR(1%,B$," ")
        \Y%=VAL(LEFT(B$,R%))
        \B$=CVT$$(RIGHT(B$,R%),8%)

3590    IF LEFT(B$,1%)="@" THEN GOTO 3700

3600    IF LEN(B$)=0% THEN 3800

3610    R%=INSTR(1%,B$," ")
        \O%=10%*VAL(LEFT(B$,R%))
        \B$=CVT$$(RIGHT(B$,R%),8%)
        \Q1=COS(O%*PI/4)\Q2=SIN(O%*PI/4)

3620    ON INSTR(1%,"GRLCVIQD",LEFT(B$,1%)) GOTO 3800,3900,3900,3900
         ,3900,3900,3950,3900

3700    Y0%=Y%\X0%=X%
        \B$=CVT$$(RIGHT(B$,2%),8%)

3710    R%=INSTR(1%,B$," ")
        \X%=VAL(LEFT(B$,R%))
        \B$=CVT$$(RIGHT(B$,R%),8%)

3720    Y%=VAL(B$)\W1%=(X%-X0%)/3%\W2%=(Y%-Y0%)/3%

3730    X%=X%-W1%\Y%=Y%-W2%\GOSUB 3800
        \X%=X%-W1%\Y%=Y%-W2%\GOTO 3800
```

```
EAGLE.BAS                    Created  16-Feb-77  at  10:36

3800    C$=FNQ$(2%)+FNN$(-10%,10%)+FNN$(10%,-10%)+FNQ$(2%)
           +FNN$(10%,10%)+FNN$(-10%,-10%)\RETURN

3900    X%=X%+Q1*12%\Y%=Y%-Q2*12%\GOSUB 3800
        \X%=X%+Q1*12%\Y%=Y%-Q2*12%\GOSUB 3800
        \X%=X%+Q1*12%\Y%=Y%-Q2*12%\GOTO 3800

3950    C$=FNQ$(2%)+FNO$(4%,16%)+FNO$(36%,-16%)+FNQ$(2%)
           +FNO$(4%,-16%)+FNO$(36%,16%)\RETURN

4000    !MENU

4010    PRINT FNQ$(2%)+FNP$(816,304)+FNQ$(1%)+"[] SAVE"

4020    PRINT FNQ$(2%)+FNP$(816,240)+FNQ$(1%)+"[] APPEND"

4030    PRINT FNQ$(2%)+FNP$(816,176)+FNQ$(1%)+"[] REDRAW"

4040    PRINT FNQ$(2%)+FNP$(816,112)+FNQ$(1%)+"[] ERASE"

4045    C$=FNT$(816%,48%,"[] EDIT")

4050    B$=FNR$\C$=FNT$(X%,Y%,B$)

4060    X%=X% AND -32%\Y%=Y% AND -32%

4065    X0%=X%\Y0%=Y%

4070    IF X%=800% AND Y%=160% THEN GOTO 9000

4080    IF X%=800% AND Y%=96% THEN E%=-1%\RETURN

4090    IF X%=800% AND Y%=288% THEN 4200

4100    IF X%=800% AND Y%=224% THEN 4300

4110    IF X%=800% AND Y%=32% THEN 4400

4120    GOTO 4000

4200    PRINT FNQ$(2%)+FNP$(800%,272%)+FNQ$(1%);\INPUT "NAME";C$

4210    OPEN C$+".CKT" FOR OUTPUT AS FILE #3%

4220    I%=VAL(S$(0%))\K%=0%\
        K%=K%+1% IF LEN(S$(J%))=0% FOR J%= 1% TO I%

4225    PRINT #3%,I%-K%

4230    PRINT #3%,S$(J%) IF LEN(S$(J%)) FOR J%= 1% TO I%

4240    CLOSE #3%

4250    RETURN

4300    !APPEND
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
4310    PRINT FNQ$(2%)+FNP$(800%,208%)+FNQ$(1%);\INPUT "NAME";C$

4320    OPEN C$+".CKT" FOR INPUT AS FILE #3%

4330    INPUT #3%,J%
        ! GET LENGTH OF ADDED PICTURE

4340    I%=VAL(S$(0%))+1%

4350    INPUT #3%,S$(K%) FOR K%=I% TO I%+J%-1%

4360    S$(0%)=NUM$(J%+I%)

4370    GOTO 9000

4400    !EDIT

4405    C$=FNQ$(0%)

4410    I1%=VAL(S$(0%))

4415    D%=0%

4420    FOR J1%=1% TO I1%

4425    IF D% THEN C$="N"\GOTO 4450

4430    A$=S$(J1%)\GOSUB 10000

4440    PRINT FNQ$(2%)+FNP$(Q3%,Q4%+15%)+FNQ$(1%);\INPUT "RETAIN";C$

4444    IF C$="NONE" THEN D%=-1%

4450    IF INSTR(1%,C$,"N") THEN GOSUB 3550\S$(J1%)=""

4452    IF INSTR(1%,C$,"ALL") THEN GOTO 4470

4460    NEXT J1%

4470    GOTO 9000
        ! REDRAW EDITED PICTURE

9000    S%=VAL(S$(0%))
        ! GET NUMBER OF CARDS

9005    C$=FNQ$(0%)
        ! RESET THE SCREEN

9010    FOR I%=1% TO S%
        ! DRAW EACH CARD

9020    A$=S$(I%)\GOSUB 10000

9030    NEXT I%
```

```
EAGLE.BAS                    Created  16-Feb-77  at  10:36

9040     RETURN

10000    IF LEFT(A$,1%)<>"@" THEN RETURN
         ! MUST BE A GRAPHIC CARD

10010    B$=CVT$$(RIGHT(A$,2%),1%+4%+8%+16%+32%)
         !DROP THE @ SIGN

10020    R%=INSTR(1%,B$," ")
         !FIND THE FIRST BLANK IN B$

10030    X%=VAL(LEFT(B$,R%))\
         B$=CVT$$(RIGHT(B$,R%),8%)
         ! GET THE X COORDINATE

10040    R%=INSTR(1%,B$," ")\
         Y%=VAL(LEFT(B$,R%))\
         B$=CVT$$(RIGHT(B$,R%),8%)
         ! GET THE Y COORDINATE

10045    IF LEFT(B$,1%)="@" THEN GOTO 10500
         ! WIRE CARD

10046    IF LEN(B$)=0 THEN GOTO 10600
         ! NODE CARD

10050    R%=INSTR(1%,B$," ")\
         O%=10%*VAL(LEFT(B$,R%))\
         B$=CVT$$(RIGHT(B$,R%),8%)
         ! GET ORIENTATION

10055    Q1=COS(O%*PI/4)\Q2=SIN(O%*PI/4)

10060    R%=INSTR(1%,B$," ")\
         T$=LEFT(B$,R%-1%)\
         B$=CVT$$(RIGHT(B$,R%),8%)
         ! GET TYPE IDENIFIER

10070    R%=INSTR(1%,B$," ")\
         K$=LEFT(B$,R%-1%)\
         B$=CVT$$(RIGHT(B$,R%),8%)
         ! GET VALUE OR KIND

10080    ON INSTR(1%,"GRLCVIQD",LEFT(T$,1%)) GOTO 10700,10800,10900,
          11000,11100,11200,11300,11400

10500    C$=FNQ$(2%)+FNP$(X%,Y%)
         ! START OF WIRE

10505    B$=CVT$$(RIGHT(B$,2%),8%)
         ! REMOVE @ SIGN AND LEADING SPACES

10510    R%=INSTR(1%,B$," ")\
         X%=VAL(LEFT(B$,R%))\
         B$=CVT$$(RIGHT(B$,R%),8%)
         ! NEXT X
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
10520    Y%=VAL(B$)
         ! NEW Y

10530    C$=FNP$(X%,Y%)\
         RETURN
         ! DRAW THE WIRE

10600    C$=FNQ$(2%)+FNN$(1%,1%)+FNN$(1%,-1%)+FNN$(-1%,-1%)+
                FNN$(-1%,1%)+FNN$(1%,1%)\
         RETURN
         ! NODE OR CONNECTION POINT

10700    ! GROUND NODE

10710    C$=FNQ$(2%)+FNN$(0,0)+FNN$(0,-4%)+FNQ$(2%)+FNN$(12%,-4%)
             +FNN$(-12%,-4%)+FNQ$(2%)+FNN$(8%,-8%)+FNN$(-8%,-8%)
             +FNQ$(2%)+FNN$(2%,-12%)+FNN$(-2%,-12%)

10720    RETURN

10800    ! RESISTOR

10810    C$=FNQ$(2%)+FNN$(0%,0%)+FNO$(8%,0%)+FNO$(12%,4%)
             +FNO$(20%,-4%)+FNO$(28%,4%)+FNO$(36%,-4%)
             +FNO$(40%,0%)+FNO$(48%,0%)

10820    IF 0%>3% THEN
           U%=12%*Q1-28%*Q2\V%=-28%*Q1-12%*Q2\GOTO 10840

10830    U%=12%*Q1+28%*Q2\V%=28%*Q1-12%*Q2

10840    Q3%=U%+X%\Q4%=V%+Y%\Q5%=Q4%-15%

10850    C$=FNT$(Q3%,Q4%,T$)+FNT$(Q3%,Q5%,K$)

10860    RETURN

10900    ! INDUCTOR

10910    C$=FNQ$(2%)+FNN$(0,0)+FNO$(12%,0%)+FNO$(16%,4%)
             +FNO$(12%,8%)+FNO$(8%,4%)+FNO$(16%,-4%)+FNO$(20%,-4%)
             +FNO$(28%,4%)+FNO$(24%,8%)+FNO$(20%,4%)
             +FNO$(28%,-4%)+FNO$(32%,-4%)

10915    C$=FNO$(40%,4%)+FNO$(36%,8%)+FNO$(32%,4%)+FNO$(40%,0%)+FNO$(48%,0

10920    GOTO 10820
         ! COMMON LABEL ROUTINE

11000    ! CAPACITOR

11010    C$=FNQ$(2%)+FNN$(0%,0%)+FNO$(20%,0%)+FNQ$(2%)+FNO$(20%,8%)
             +FNO$(20%,-8%)+FNQ$(2%)+FNO$(32%,-8%)+FNO$(28%,-4%)
             +FNO$(28%,4%)+FNO$(32%,8%)+FNQ$(2%)+FNO$(28%,0%)+FNO$(48%,0%)
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
11020   GOTO 10820
        ! COMMON LABELING ROUTINE

11100   ! VOLTAGE SOURCE

11110   C$=FNQ$(2%)+FNN$(0%,0%)+FNO$(12%,0%)+FNQ$(2%)

11120   C$=FNO$(12%*SIN(A)+24%,12%*COS(A)) FOR A=0 TO 2*PI+.1 STEP

11130   C$=FNQ$(2%)+FNO$(8%,12%)+FNO$(8%,4%)+FNQ$(2)
            +FNO$(4%,8%)+FNO$(12%,8%)+FNQ$(2%)+FNO$(36%,0%)
            +FNO$(48%,0%)

11140   GOTO 10820
        ! GOTO COMMON LABLE ROUTINE

11200   ! CURRENT SOURCE

11210   C$=FNQ$(2%)+FNN$(0%,0%)+FNO$(8%,0%)+FNQ$(2%)

11220   C$=FNO$(12%*SIN(A)+20%,12%*COS(A)) FOR A= 0 TO 2*PI+.1 STEP

11230   C$=FNQ$(2%)

11240   C$=FNO$(12%*SIN(A)+28%,12%*COS(A)) FOR A= 0 TO 2*PI+.1 STEP PI/

11250   C$=FNQ$(2%)+FNO$(36%,0%)+FNO$(12%,0%)+FNO$(14%,-4%)
            +FNQ$(2%)+FNO$(12%,0%)+FNO$(14%,4%)+FNQ$(2%)
            +FNO$(40%,0%)+FNO$(48%,0%)

11260   GOTO 10820

11300   ! BIPOLAR TRANSISTORS

11310   C$=FNQ$(2%)+FNN$(0%,0%)+FNO$(12%,0%)+FNQ$(2%)+FNO$(12%,20%)
            +FNO$(12%,-20%)+FNQ$(2%)+FNO$(12%,12%)+FNO$(32%,32%)+FNQ$(2%)
            +FNO$(12%,-12%)+FNO$(32%,-32%)

11320   IF (INSTR(1%,Q5$,K$+"#") AND Q%=4) THEN
        C$=FNQ$(2%)+FNO$(24%,-20%)+FNO$(20%,-20%)+FNO$(20%,-24%)

11330   IF (INSTR(1%,Q5$,K$+"#") AND Q%=0%) THEN
        C$=FNQ$(2%)+FNO$(24%,20%)+FNO$(20%,20%)+FNO$(20%,24%)

11340   IF (INSTR(1%,Q6$,K$+"#") AND Q%=4%) THEN
        C$=FNQ$(2%)+FNO$(24%,20%)+FNO$(24%,24%)+FNO$(20%,24%)

11350   IF (INSTR(1%,Q6$,K$+"#") AND Q%=0%) THEN
        C$=FNQ$(2%)+FNO$(24%,-20%)+FNO$(24%,-24%)+FNO$(20%,-24%)

11380   Q4%=Y%\Q5%=Q4%-15%\
        IF Q%>3% THEN Q3%=X%-96% ELSE Q3%=X%+32%

11390   GOTO 10850
        ! PRINT LABEL
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
11400   ! DIODE

11410   C$=FNQ$(2%)+FNN$(0,0)+FNO$(20%,0%)+FNO$(20%,8%)
           +FNO$(28%,0%)+FNO$(20%,-8%)+FNO$(20%,0%)+FNQ$(2%)
           +FNO$(28%,8%)+FNO$(28%,-8%)+FNQ$(2%)+FNO$(28%,0%)
           +FNO$(48%,0%)

11420   GOTO 10820
        ! COMMON LABEL ROUTINE

19000   PRINT FNQ$(1%)\RESUME 19100

19100   W8%=ERR\W9%=ERL

19110   STOP

20010   DEF FNN$(U%,V%)=FNP$(X%+U%,Y%+V%)
        ! FUNCTION TO DO TRANSLATION OF POINT

20020   DEF FNO$(U%,V%)

20030   Q0=U%\U%=U%*Q1+V%*Q2\V%=V%*Q1-Q0*Q2

20040   FNO$=FNN$(U%,V%)

20050   FNEND

20060   !

20070   DEF FNP$(X%,Y%)
        ! THIS FUNCTION IS USED TO DRAW A VECTOR FROM THE
          PREVIOUS POINT SPECIFIED TO THE POINT AT X%,Y%
          THE FIRST VECTOR AFTER A MODE COMMAND(FNQ$)
          IS NOT DISPLAYED

20080   LSET V$=CHR$(32%+(Y%/32% AND 31%))+CHR$(96%+(Y% AND 31%))+
                CHR$(32%+(X%/32% AND 31%))+CHR$(64%+(X% AND 31%))
        ! CONVERT CO-ORDINATES TO TEK FORMAT

20090   PUT #1%,RECORD 1%,COUNT 4%
        ! DRAW THE VECTOR

20100   FNP$=""
        ! NULL VALUE TO FUNCTION

20110   FNEND
        ! END OF PLOT FUNCTION

20120   !

20130   DEF FNQ$(Q%)
        ! THE FUNCTION FNQ$ IS USED TO ESTABLISH THE MODE OF THE
          GRAPHICS TERMINAL. E.G. A$=FNQ$(0%) WILL ERASE THE SCREEN

20140   !
         FNQ$(0%) ERASES THE SCREEN AND PUTS THE TERMINAL IN ALPHA MODE
```

```
EAGLE.BAS                    Created  16-Feb-77  at  10:36

          FNQ$(1%)                          PUTS THE TERMINAL IN ALPHA MODE
          FNQ$(2%)                          PUTS THE TERMINAL IN GRAPH MODE
          FNQ$(3%) USED BY FNR$ FOR GRAPHIC INPUT MODE

20150     IF Q%=0% THEN OPEN "KB:" FOR OUTPUT AS FILE 1%\
          FIELD #1%,64% AS V$
          ! OPEN FOR GRAPHICS AT START UP

20160               IF Q%=0% THEN LSET V$=CHR$(27%)+CHR$(12%)
          ELSE      IF Q%=1% THEN LSET V$=CHR$(27%)+CHR$(31%)
          ELSE      IF Q%=2% THEN LSET V$=CHR$(27%)+CHR$(29%)
          ELSE      IF Q%=3%THEN LSET V$=CHR$(27%)+CHR$(26%)

20170     PUT #1%,RECORD 1%,COUNT 2%
          \IF Q%=0% THEN SLEEP 2%
          ! CHANGE MODE, WAIT IF ERASE FUNCTION

20180     FNQ$=""
          ! NULL VALUE TO FUNCTION

20190     FNEND
          ! END OF MODE SET FUNCTION

20200     !

20210     DEF FNR$
          ! FUNCTION TO ACQUIRE THE CORDIANTES OF THE CROSS HAIRS

20220     !
          FNR$ HAS NO ARGUMENT; RESULT IS THE CHARACTER TYPED BY THE
          USER; AFTER FNR$ THE TERMINAL IS IN THE ALPHA MODE AND THE
          COORDINATES OF THE CROSS HAIRS ARE LEFT IN GLOBAL VARIABLES
          X% AND Y%

20230     OPEN "KB:" FOR INPUT AS FILE 2%
          ! PREPARE TO GET CROSS HAIRS

20240     W$=SYS(CHR$(3%)+CHR$(2%))+FNQ$(3%)
          ! SINGLE CHARACTER INPUT,TURN ON CROSS HAIRS

20250     FIELD #2%,10% AS U$
          ! SETUP INPUT BUFFER

20260     X$=""
          \X%=0%
          ! INITIALIZE WORKING VARIABLES

20270     W$=SYS(CHR$(4%)+CHR$(2%))
          \GET #2%,RECORD 1%
          ! NO WAITING FOR DATA,GET WHAT YOU CAN

20280     X$=X$+LEFT(U$,RECOUNT)
          ! GET THE NEW STUFF

20290     X%=X%+RECOUNT
          ! COUNT HOW MANY WE GOT
```

EAGLE.BAS Created 16-Feb-77 at 10:36

```
20300   IF X%<5% THEN GOTO 20270
        ! LOOP UNTIL WE GET IT ALL

20310   W$=SYS(CHR$(2%)+CHR$(2%))
        \CLOSE 2%
        ! FINISH UP THE TRANSFER

20320   CHANGE X$ TO X%
        ! CONVERT CHARACTERS TO NUMERICS,DEFORMAT TEK

20330   X%=32%*((X%(2%) AND 31%)-32%)+(X%(3%) AND 31%)+1023%
        ! X COORDINATE AS A NUMBER

20340   Y%=32%*((X%(4%) AND 31%)-32%)+(X%(5%) AND 31%)+1023%
        ! Y COORDINATE AS A NUMBER

20350   FNR$=CVT$$(LEFT(X$,1%),32%)
        ! UPPER CASE CHARACTER AS TYPED

20360   FNEND
        ! END OF READ CROSSHAIR

20370   DEF FNT$(U%,V%,T$)
        ! FUNCTION TO PRINT TEXT T$ AT U%,V% ON SCREEN

20380   PRINT FNQ$(2%)+FNP$(U%,V%)+FNQ$(1%)+T$
        ! DO IT TO IT

20390   FNEND
        ! END OF DISPLAY TEXT

32766   PRINT FNQ$(1%)

32767   END
        ! REALLY
```

Part 9

Computer Aided Design Survey

Prepared for

U. S. Army Missile Command

Redstone Arsenal, Alabama

Under Contract

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by

Electrical Engineering Department
Auburn University
Auburn, Alabama

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Alumni Professor

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INTRODUCTION

The list of disciplines impacted by the digital computer is growing at an increased rate. The developers of the first electronic computer, the ENIAC could not have imagined the many applications of the descendants of their "work." Some of the present technologies were not even in existence then. Significant among these technologies are computer graphics and computer-aided-design. Computer-aided-design systems (most often with computer graphics capability) coupled with a knowledgeable user constitute a man-machine combination markedly superior to either of them acting independently. Such a team is not only capable of doing "standard" tasks more quickly, it can accomplish jobs that were here-to-fore impractical if not impossible. Precipitious drops in hardware costs coupled with increased usage have resulted in the availability of hardware suitable for a fairly sophisticated system for under $50,000. The cost of commercially available systems including graphics software is significantly higher.

The potential of computer graphics has been recognized within the microelectronics branch of AMICOM. Several years ago, an interactive CAD system was installed. Its use has been extensive in the preparation of artwork for thick film hybrid microelectronic circuits, printed circuit boards, and fluidic devices. However, several deficienceis have kept the system from realizing its attainable capacity. Perhaps its most serious deficiency is its inability to assist the user in resolving

design problems that are more complicated than the placing of components and routing of conductors. In fact the problems of placement and routing where hundreds of components and conductors are involved is far from trivial since these procedures are not automated. Layout influences the eventual maximum temperatures in the circuit and its supporting substrate. Improper routing of conductors can lead to undesirable feedback and crosstalk. Clearly the design of a hybrid microelectronic circuit involves much more than the evolution of a schematic and its implementation on a small piece of substrate. Many of the associated tasks are tedious and time consuming. Fortunately some can be done by computer; computer assistance in addition to computer graphics is desirable.

Numerous computer-aided-design systems for electronic circuits have been developed in university, governmental, and industrial laboratories. Many are capable of widespread application, but no known system addresses itself specifically to the problems of thick film hybrid microelectronics. This section describes the overall concept of computer-aided-design and surveys available CAD programs which might be used at AMICOM.

ELECTRONIC CIRCUIT DESIGN

Development of microelectronic technologies has had a major impact on the process of designing electronic circuits. A decade ago designers had at their disposal discrete components such as transistors, diodes, resistors, capacitors, inductors, and others, plus a few models of small-scale integrated-circuits. Component interconnections were made using discrete wiring or printed circuit boards. Today a designer has in addition to the above, components such as medium and large scale integrated circuits of several technologies. Furthermore, passive components such as resistors and capacitors can be constructed using thin or thick film techniques which permits the fabrication of hybrid circuits containing combinations of discrete components, integrated circuits, and thick or thin film components in the same package. Interconnection techniques now available include printed circuit boards, wire-wrap planes, discrete wiring, thick film substrates, thin film substrates, and monolithic substrates. These complex components and dense packaging and interconnection techniques have increased the capability of electronic circuits and have magnified the problems of circuit designers. Design aspects that have been made significantly more difficult are design verification, circuit analysis, physical design, and testing. Computer aided design methods are being developed to enable the design engineer to solve these problems in a cost-effective and time-effective manner.

The steps given below represent an outline of the process for designing and fabricating a complex electronic circuit. See Figure 1. It is important to understand that during the process it often becomes necessary to return to earlier steps in the process. Hence, the process is iterative.

1. Formulate a preliminary circuit design - This step is performed by a design engineer using his intuition and knowledge of the circuit specifications and of the available components and packaging techniques.

2. Validate the preliminary design - Design validation is a difficult and important step where computer-aided design tools can be effectively utilized. Valuable design tools include circuit analysis programs and logic simulation programs. Such programs can be used to evaluate a circuit design without the need for construction of a prototype circuit. However, construction and testing of a prototype should be considered when feasible. When prototype construction is not feasible it is imperative that the computer analysis be thorough and accurate.

3. Make an implementation decision - This step represents the start of the physical design of the circuit. Possible choices include standard modules on printed circuit boards, hybrid microcircuits with either standard or custom components, or customized integrated circuits. Factors influencing the decision are schedules, quantity, size, power, g-factors, cost, and others.

4. Partition the circuit design into physically realizable components - Automation of this step is difficult and is most effectively accomplished by a design engineer using his knowledge of available standard components and of feasible custom components.

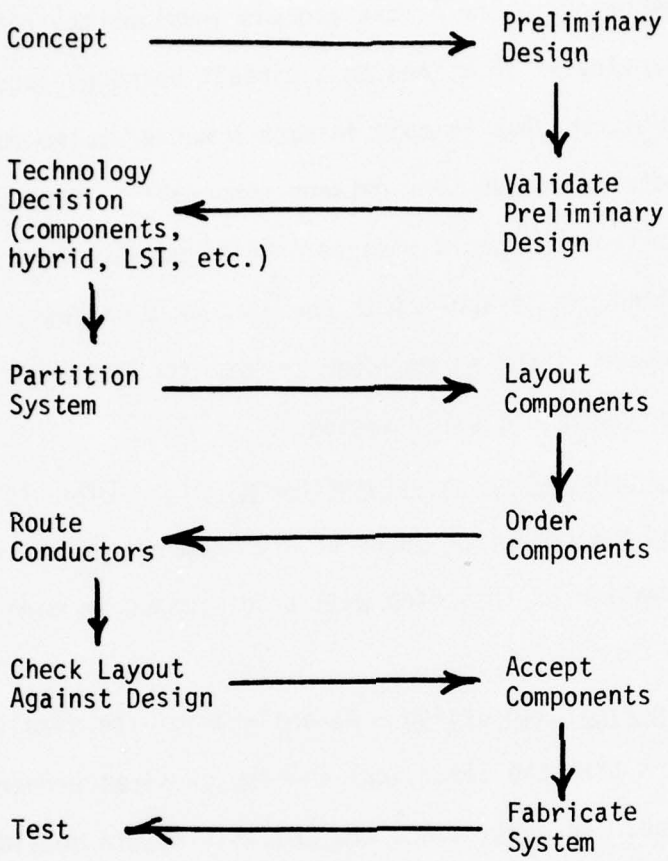

Figure 1. General electronic circuit implementation process.

5. Procure components.

6. Layout components - The layout process involves the placement of components at particular locations on a circuit board or substrate. Placement is not arbitrary but is made in such a manner as to facilitate the routing of electrical conductors between components. Heat buildup and electrical interference should also be considered when making component placement. Automation can be applied to the placement process, but the most effective approach is for an engineer to make the placement with the aid of a computer driven display system.

7. Route the conductor paths between components - This step determines the exact routing of all conductor paths between components on the board or substrate. Automation of this step will be discussed in more detail in a later section.

8. Analyze the finalized design - An analysis of the finalized design that considers both the electrical and the physical properties of the circuit is needed. In particular, the analysis should consider loading, power, coupling, interference, noise, and heating characteristics of the circuit. Computer analysis programs can be effectively used in this step.

9. Perform acceptance on all procured components - Automation can be used here for selecting test patterns and for performing the actual testing of components.

10. Fabricate the final circuit - Automation is extensively used at this step in the production of masks, etc.

11. Test the final circuit - Automation can be applied here as in step 9.

The generalized electronic circuit implementation described above may be tailored somewhat for different circuit types. For example, Figure 2 shows an expanded version of Figure 1. The figure is for both analog and digital logic circuits. The technology decision is usually based on several factors: project schedule; quantity of circuits needed; environmental factors such as size, weight, temperature, humidity, g-factors, etc.; cost limitations, power requirements, and many others. The details of hybrid substrate and custom LSI chip implementation are displayed in Figures 3 and 4.

The implementation process of Figures 1, 2, 3, and 4 implies that a team of designers and technicians are performing the listed tasks. If portions of the process can be computer-aided, the design and production time can be greatly reduced. For example, a design automation system is outlined in Figure 5. This system, under computer control, would perform all of the initial system design functions and automatically generate a circuit level implementation.

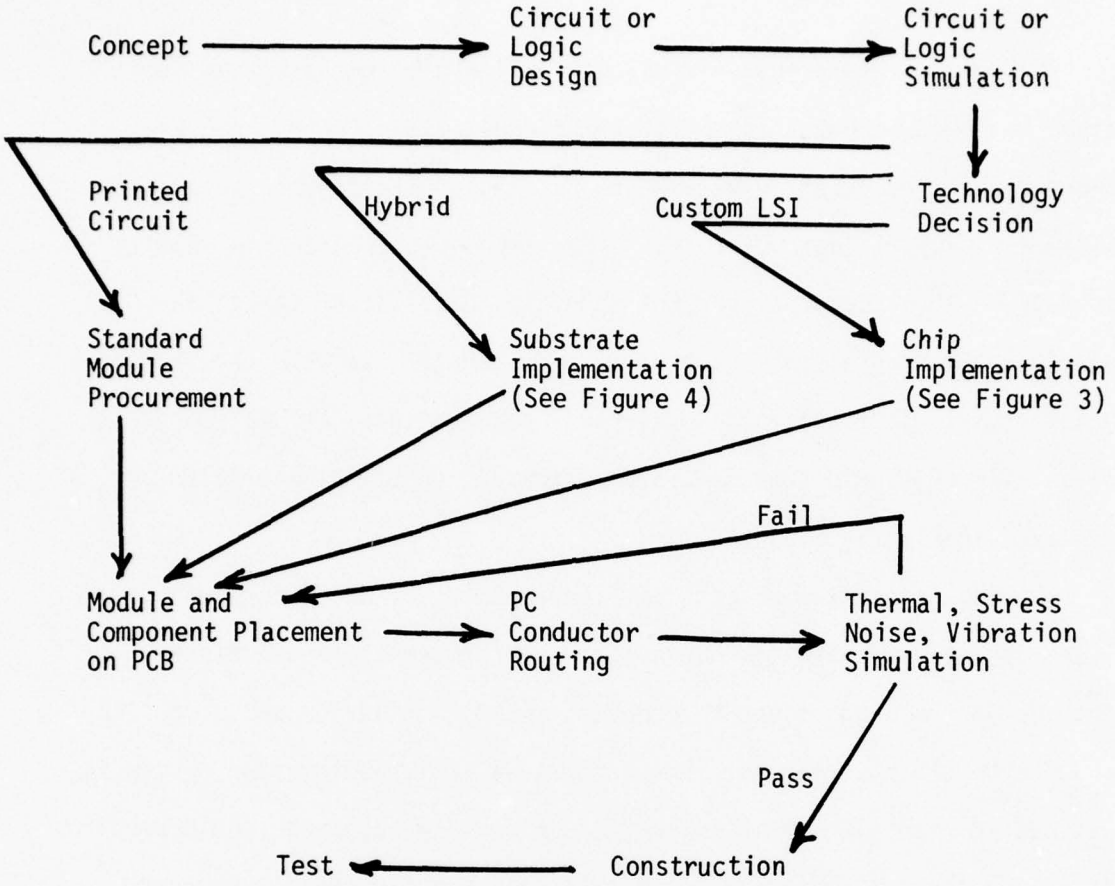

Figure 2. Expanded circuit implementation

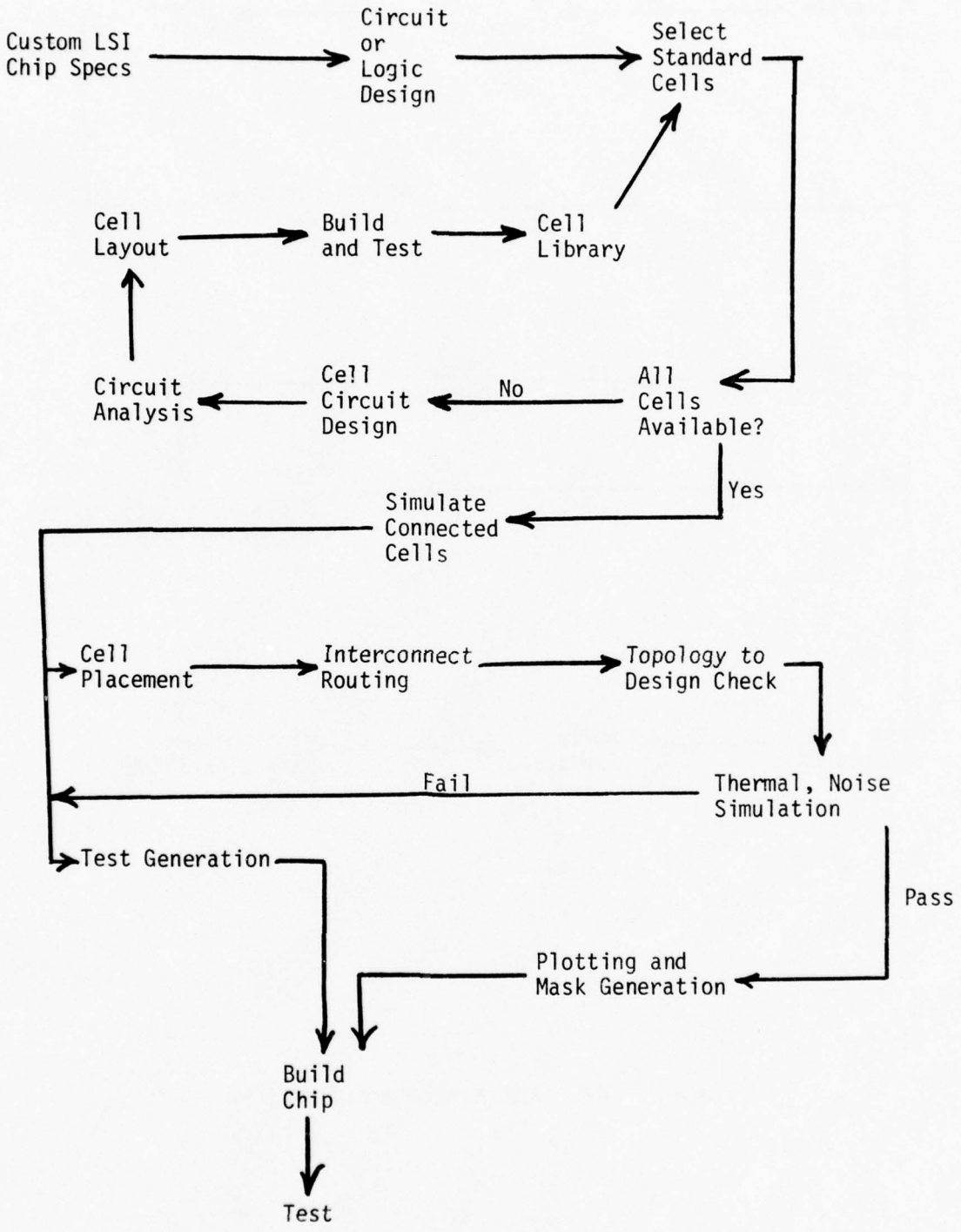

Figure 3. Custom LSI Chip Implementation

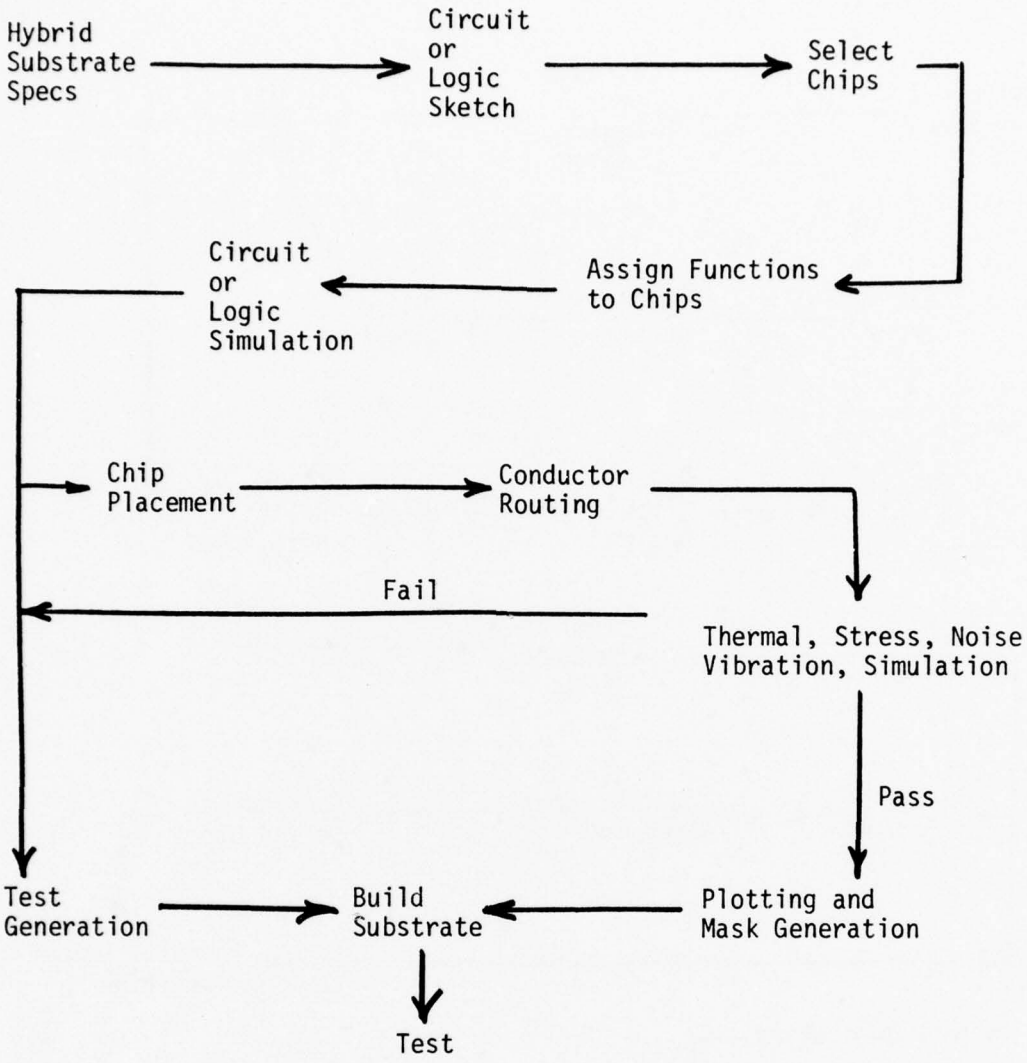

Figure 4. Hybrid Substrate Implementation

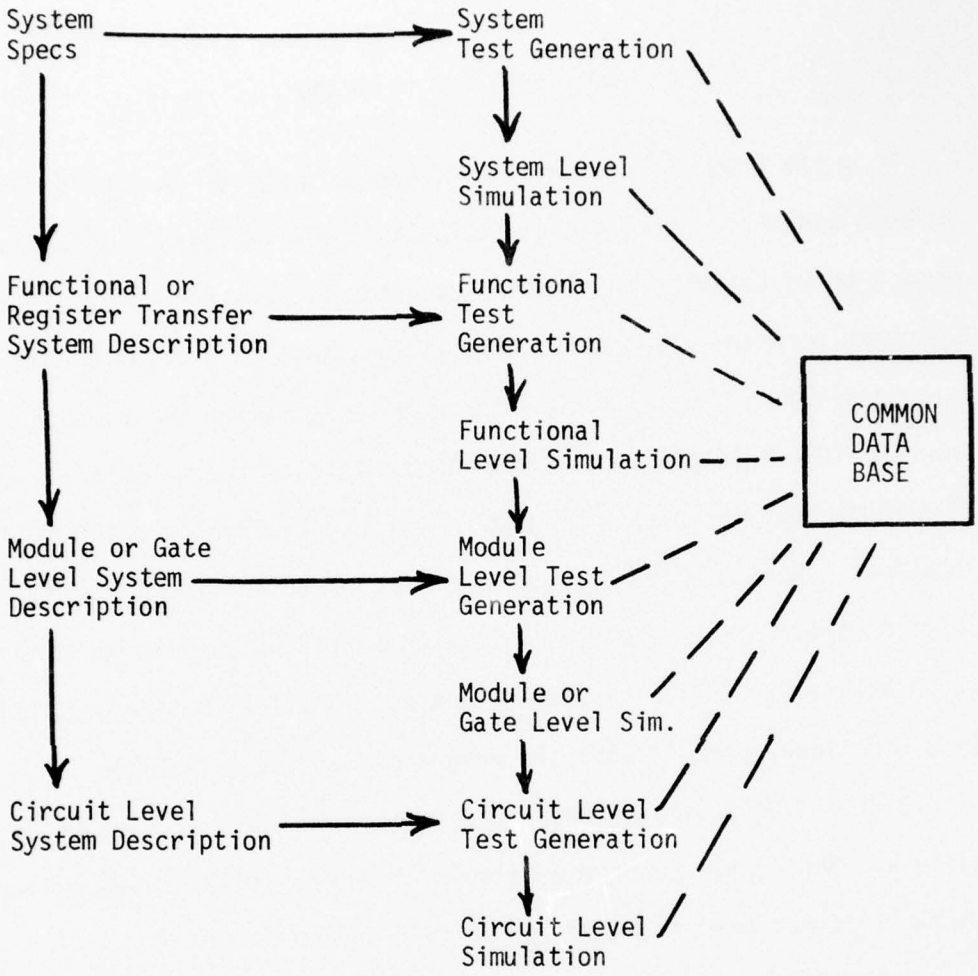

Figure 5. Design Automation

AVAILABLE CAD PROGRAMS

Many CAD programs are available, and in use, for the design and implementation of analog and digital electronic circuits. Appendix A gives a brief description of a few programs [1] and Appendix B describes how other programs are used at typical locations around the country. In this section, several tables are used to summarize the various programs that have been identified during this survey. Table 1 lists 27 circuit analysis programs which have been developed at various locations. Auburn University uses ISPICE and ECAP. The U.S. Army Missile Command uses ECAP and NEDAP. Table 2 compares the outputs of several of these programs. ISPICE has better general application than does ECAP. Some additional circuit analysis programs are listed in Table 3.

Digital logic simulations and/or test generators are presented in Table 4. The LOGSIM program available at NASA's Marshall Space Flight Center does not operate properly for many design needs.

Table 5 lists two available schematic layout programs. Others are surely available; however, no others were readily available to the project personnel.

Topological and automated drafting programs and system are abundant. Table 6 lists a few of the accessible ones. The major difficulty with some of these systems, for example IGDS-7, is that they do not allow tolerance checks and the command structure is not tailored especially for electronic circuit mask generation.

Table 1. Circuit design programs [2].

Program Name	Type of Analysis		Statements (x 1000)	Core Requirements (K bytes)	
	Linear	Nonlinear			
ADA 74	x	x	4	64	GE
ANP 3	x		4	80-135	Tech. Univ. Denmark
ASTAP	x	x	60	200	IBM
BELAC	x		10	120	GE
CIRCUS 2	x	x	18	180-600	Boeing
COMPACT	x		2.5	96	----
CORNAP	x		3	80-110	Cornell Univ.
ECAP 2	x	x	25	200-300	IBM
EXHOPT	x		1.5	250	Columbia Univ.
IMAG 2	x	x	10	100	Honeywell-Bull,France
ISPICE	x	x	25	330	National CCS
ITRAC 3	x	x	7	120	Berne Elect.
LISA	x		17	140	IBM
MARTHA	x			32	MIT
MOFRAN	x		4	156	Same as ANP3
NAP 2	x	x	6.5	104-250	Same as ANP3
NET 2	x	x		70	GE Tempo
NICAP	x	x	10	300-250	Bell Labs
PTNA	x		1.5	64	Univ. of Ill.
SCAP	x		1.4	12	Columbia Univ.
SCEPTRE	x	x	30	228	Air Force Weapons Lab
SLICE	x	x	10	200	UC, Berkeley
SNAP	x		1.5	26	Purdue Univ.
SPICE 1	x	x	10	184	UC, Berkeley
SPICE 2	x	x	13	135 up	UC, Berkeley
SUPER SCEPTRE	x	x	40	238	Univ. Sou. Fla.
SYSCAP 2	x	x	20	60-155	Rockwell Intl.

Table 2. Circuit design program output details [2].

Program Name	Element Volts	Node Volts	Element Current	Voltage Differences	Poles and Zeros	Transfer Function	Gain	Driving Point Function	Group Delay	Phase
ADA 74										
ANP 3					x	x	x	x	x	x
ASTAP	x	x	x	x	x	x	x	x		
BELAC	x	x	x	x	x	x	x	x	x	x
CIRCUS 2	x	x	x	x						
COMPACT						x	x	x		x
CORNAP	x	x	x	x	x	x	x	x	x	x
ECAP 2	x	x	x	x	x					
EXHOPT	x	x	x	x	x		x	x		x
IMAG 2	x	x		x	x	x	x			x
ISPICE	x	x	x	x	x	x	x			x
ITRAC 3	x	x	x							
LISA	x	x	x	x	x	x	x	x	x	
MARTHA	x	x	x	x	x	x	x	x		x
MOFRAN	x	x	x	x	x	x	x	x		x
NAP 2	x	x	x	x	x	x	x	x		x
NET 2	x	x	x			x	x	x		x
NICAP	x	x	x				x			
PTNA	x	x	x			x	x			
SCAP	x		x	x	x					
SCEPTRE	x		x							
SLIC		x	x			x	x	x		x
SNAP		x		x	x	x		x		
SPICE 1		x	x	x	x	x	x	x		x
SPICE 2		x	x	x	x	x	x	x		x
SUPER SCEPTRE	x	x	x	x	x					
SYSCAP	x	x	x	x	x		x			x

Table 3. Additional circuit design programs [3].

ACRONYM	USING ORGANIZATION
AEDCAP	Raytheon
ALCAP	Rockwell International
ASAP	IBM
CIRC	Silicon Systems, Inc.
DCNL	Collins Radio
DICAP	Rockwell International
FETSIM	RCA
FVAPC5	Collins Radio
MOSTRAN	Honeywell
MSINC	Stanford University
NEDAP	Army Missile Command
PVAPC5	Collins Radio
RCAP	RCA
RECAL	RCA
SNAP	National Semiconductor
TESS	TRW
TRAC	Silicon Systems, Inc.
TRACAP	Rockwell International
TRANT	Advanced Memory Systems
UCCAP	Harris Semiconductor
WCAC5	Collins Radio

Table 4. Available logic simulation programs [3].

ACRONYM	USING ORGANIZATION
DIGISAT	Hughes Aircraft Company
D-LASAR	United Aircraft
FAIRSIM	Fairchild Semiconductor
FANSIM	Sylvania
G-LASAR	Grumman
HAL1900	Philco Ford
LASAR	Lockheed-Georgia
LATS	General Electric
LOGCAP	Harris Semiconductor
LOGIC	Westinghouse, TRW
LOGICBLOSSOM	Harris Semiconductor
LOGICS	Auburn University
LOGICSPEC	Singer-Kearfott
LOGSIM	NASA-Marshall Space Flight Center
SALOGS	Sandia Laboratories
SIMPAC	Sperry Univac
SIMSTRAN	Rockwell International
SIMULATOR	Raytheon
TEGAS	Naval Weapons Laboratory
TIBSD	Texas Instruments

Table 5. Available schematic generation programs

ACRONYM	USING ORGANIZATION
GAIN	Sandia Laboratories
EAGLE	Auburn University

Table 6. Available Topological Systems.

SYSTEM	USING ORGANIZATION
CSSL	Draper Laboratories
SAL	Sandia Laboratories
Applicon	Sandia Laboratories
IGDS-7	M & S Computing
Computervision	NELC
Macrodata	Martin-Orlando
Calma	Harris Semiconductor

Finally, Table 7 lists a few component placement and/or conductor routing programs. These programs are generally very large and require a very competent design/engineer to use them successfully.

Table 7. Available placement/routing programs [3].

ACRONYM	PLACE	ROUTE	TECHNOLOGY	USING ORGANIZATION
AEWRAP	no	yes	Wire-Wrap	RCA
AIDS	yes	yes	Multi-Layer PC	General Electric
APAR	yes	yes	MOS LSI	Sandia Laboratories
AUTODRAFT	yes	yes	Hybrids	RCA
CARI	no	yes	Hybrids	Raytheon
GWRAP	---	yes	Wire-Wrap	General Electric
MULTI	---	yes	Multi-Layer PC	Westinghouse
PCCARDS	yes	yes	2-Layer PC	Harry Diamond Labs
PLINT	yes	yes	MOS LSI	General Electric
PRF	yes	yes	MOS LSI	National Security Agency
REDAL	yes	yes	2-Layer PC	Boeing
SCI-CARDS	yes	yes	Multi-Layer PC	Martin - Orlando
WIRE	---	yes	Wire-Wrap	Westinghouse

RECOMMENDATIONS

Currently, AMICOM is undergoing a vast reorganization. Generally speaking, the programs listed in Table 8 are recommended as target goals for AMICOM. The implementation of most of these programs, in an interactive mode, requires a direct data communication link to the CDC6600 from the PDP 11/40, as well as ready access to a remote job entry station. Since AMICOM is reorganizing and planning to install a second CDC6600, an implementation plan [4] can not be completed at this time. However, it can be stated that a direct link from the hybrid microcircuit facility to a CDC6600 is essential to the successful implementation of any CAD system, and that high-priority, interactive access to said CEC6600 is prerequisite.

Table 8. Suggested CAD Programs.

CAD Program Type	Suggested Acquisition
Interactive Layout-Hybrids	IGDS-7
Circuit Analysis	ISPICE
Thermal Analysis	CINDA
Logic Simulation	LOGICS
Interactive Schematic	EAGLE
Multilayer P.C. Routing	SCI-CARDS
Vibration and Stress	NASTRAN
Noise Analysis	N/A
LSI Layout	Upgrade of NASA-MSFC System

REFERENCES

[1] CAD/CAM

[2] G. Kaplan, "Computer-Aided Design," IEEE Spectrum, Vol. 12, October 1975, p. 40.

[3] P. R. Owens, et.al., "Computer Aided Design for Electronics in 1975," Survey Report, Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio, 1975.

[4] H. T. Nagle, Jr. and J. Knaur, "Hybrid Microelectronic Computer-Aided-Design Project," Summary Report, Battelle Laboratories, 1975.

[5] M. A. Breuer, "Recent Developments in the Automated Design and Analysis of Digital Systems," Proc. IEEE, Vol. 60. Jan. 1972, p. 12.

[6] A. Bolopion, et.al., "A New Approach to CAI by Interactive Design of Electrical Engineering Systems," IEEE Trans. Education, Vol. E-18, May, 1975, p. 87.

[7] M. C. van Lier and P. H. J. M. Otten, "Automated IC Layout: The Model and Technology," IEEE Trans. Circ. and Systems, Vol. CAS-22, November, 1975, p. 845.

[8] G. Szentirmai, ed., Computer Aided Filter Design, IEEE Press, 1973.

[9] H. Falk, "Design for Production," IEEE Spectrum, Vol. 12, October, 1975, p. 48.

APPENDIX A

Some CAD Program Descriptions [1].

COMPUTER-AIDED DESIGN AND ENGINEERING

Ira W. Cotton
National Bureau of Standards

Objective: Assisting ECOM in the utilization and performance measurement of its computer graphics design terminal test bed system at Fort Monmouth.

Scope: NBS has assisted in connecting this system to the ARPA network through special interfaces at NBS, and will continue to refine and improve the present configuration. Performance criteria, performance measurement, and new tools (including both hardware and software) will be developed to help determine the best systems configuration to support interactive graphics in laboratory environments. Assistance will also be provided in the area of network and graphics protocols and standards.

Methodology: The ECOM facility was connected to the ARPA network via a dial-up line connected to the NBS PDP-11 minicomputer which is a host on the ARPA network Terminal Interface Processor (TIP) at NBS. Since a communications protocol was already implemented in the PDP-11 for a Univac DCT2000 terminal, programs were written at ECOM to mimic that terminal. This technique has enabled ECOM to utilize facilities such as a large IBM 360 running the NASTRAN program for structural analysis. Plans are being considered to enable ECOM to connect to the ARPA network directly as a very distant host by writing a network control program for the minicomputer in the ECOM test bed.

Status: The study began in 1970 and will continue through June 1974.

Hardware/Software:
At ECOM: Computer (Varian 620)
Display processor (IDIIOM)

At NBS: Computer (PDP-11)
Access to ARPA network through TIP

Publications: NBSIR 73-217, "Use of Computer Networks in Support of Interactive Graphics for Computer-Aided Design and Engineering," National Bureau of Standards, 1973.

WIRING DESIGN AUTOMATION SOFTWARE

James H. Haynes
University of California

Objective: A family of computer programs to aid wiring design. Our research and teaching require the construction of digital systems, computer accessories, and similar hardware. Our usual method of construction is based on integrated circuits mounted in sockets and interconnected with wrapped wiring.

Scope: The principal value of automated wiring design for one-of-a-kind equipment is that it allows the use of pre-cut and stripped wire, at a great saving in construction time over hand cutting and stripping. Additionally, the programs reduce the effort involved in creating a wire list, minimize wire length, and provide printed lists in various formats.

Methodology: Input to the system is through a program which minimizes keystrokes. A keypunch operator is trained to punch directly from logic schematics proepared by the engineer; or the latter may do his own keypunching. The information is expanded to one record per pin to be wired. These records are sorted by pin number to permit detection of duplicate names on pins, and printed. Then the records are sorted by logic name, to bring together all pins to be wired together. The next program, using a table of information about the geometry of the mounting board, calculates a minimum-length wiring path for each net, constrained to a maximum of two wires per pin. This is printed. Then the pin-to-pin wiring records are sorted into the optimum order for wiring and printed in that format for the operator who does the wiring.

Status: Programs are *debugged*, *documented* and in use. Future plans are to write additional programs to aid in modifying existing wire lists and equipment.

Hardware/Software: Computer (IBM 360/40 with 256K core under OS-HASP)
Sort-merge utility
PL/1

Publications: Programs available from author for the cost of duplication.

Keywords: Wrapped Wiring
Pin-to-pin Wiring Records

GRAPHICAL CONTINUOUS SYSTEM SIMULATION LANGUAGE

Travis L. Herring
U.S. Naval Weapons Laboratory

Objective: A general-purpose tool for scientific computation using interactive computer graphics. Special attention was to be given to providing facilities for the modeling of physical systems and solving ordinary differential equations. Simulation-controleld animation was to be provided.

Scope: The completed system is usable by all professional technical personnel and requires little training. It is completely interactive. Plotting curves and producing animated pictures of entities under simulation is made easy by the design of the system. An interactive graphic language is provided which is close to FORTRAN but simplifies the solution of problems involving ordinary differential equations.

Methodology: A continuous system simualtion language modified ro run as an interactive grpahics program, the system was designed to handle a wide range of user sophistication. Complete error recovery is provided so that the user can correct errors and continue.

Status: This language is a proprietary product called CSSL III. A batch version of CSSL III is available. Hardcopy output of graphs and tables can be obtained.

Hardware/Software: Computers (CDC 6000 series) running under SCOPE 3.3
Graphics terminals (CDC 274/1700)
Lightpen
(8K) Refresh buffer

Publications: Travis L. Herring, "User's Guide to Graphical CSSL-A New Tool for Computation Using Interactive Computer Grpahics," NWL TR2905, January, 1973.

Related Studies: Travis L. Herring, "A User's Guide for OLDAS-An On-Line Digital Analog Simulator," NWL TR2257, January 1969.

CSSL III User's Guide/Reference Manual, Programming Sciences Corporation, 1900 Avenue of the stars, Los Angeles, California 90067, January 1971.

DESIGN AUTOMATION OF DIGITAL COMPUTERS

Melvin A. Breuer
University of Southern California

Objective: To develop new algorithms and evaluate their performance, relative to problem of design and implementation of digital systems. Our overall goal is the development of an interactive design automation system that will allow a designer to implement a system in an efficient and accurate manner.

Scope: We have investigated the following problems: (1) register transfer languages and a multitude of applications for such a language; (2) logic synthesis; (3) selection of components; (4) functional partitioning of logic circuits; (5) assignment; (6) placement; (7) logic simulation; (8) test generation. Programs implementing a number of our algorithms have been written. Our most successful program dealt with the automatic generation of fault detection tests of sequential circuits.

Methodology: Most of our problems deal with finite combinational problems. Many of these are expressed in graph-theoretic terms. Because of their complexity, heuristic solutions are often sought. The problems dealing with logic simualtion and test generation require study of modeling techniques as well as analysis of fault modes.

Status: These long-term basic and applied research studies are on-going.

Publications:

Melvin A. Breuer, "A Random and an Algorithmic Technique for Fault Detection Test Generation for Sequential Circuits," IEEE Trans. on Computers, C-20, 1364-1371, 1971.

Melvin A. Breuer, "Recent Developments in Design Automation," IEEE Computer, 23-35, 1972.

ON-LINE LOGICAL SIMULATION (OLLS) SYSTEM

Richard M. Tavan
Charles Stark Draper Laboratory, Inc.

Objective: Fast, precise system documentation and accurate logic simulation to improve the design process.

Scope: The "On-Line Logical Simulation System" (OLLS) is a complete software package which permits a logic designer to interactively design, layout and simulate large digital systems using the IBM 2250 CRT. The user communicates with OLLS through a set of interactive displays using the lightpen, keyboard and programmed function buttons. The major subsystems include file handling, device definition, drawing manipulation, simulation and input-output. OLLS is uniqu in its freedom of device definition, generality and adaptability.

Methodology: OLLS aids the logic designer in laying out, simulating, documenting and fabricating digital systems. Its major subsystems include file management, device definition, drawing manipulation, simulation and input-output. The device definition program places no restrictions on the number, ship or complexity of the logical building blocks. It includes a variety of drawing aids such as tracking symbols and symmetry axes and a copy facility that eliminates most of the tedium of initializing large glossaries. The drawing display provides variable scale and window position, allows easy signal routing and avoids many common restrictions, such as requisite names, by using consistent default conventions. Drawing plots inlcude complete frame and title blocking, the format of which is controllable. A user may logically interconnect any subset of drawings in his file to function as an integrated system. This process is very fast and lends itself to frequent reuse. The drawing and device descriptions themselves drive the simulator subsystem. The simulator currently provided is time-directed. Its use is interactive and imposes no additional constraints on device complexity or system size. It supports wired logic, variable delays, internal variables, "power-on" sequencing and simulation-only patches. Device behavior is specified for simulation purposes by standard Boolean equations using a unique (optional) syntactical convention for specifying the delay and required-time-on effects of each input, output and internal variable on each output and internal variable. In this way, the highly complex logical behavior of MSI devices may be realistically modeled. A consistent punch-card format for input and output of drawing descriptions and simulation data allows optional off-line preparation and modification of data. OLLS provides a complete set of high-speed-printed listings of the data file and plots of drawings and simulation results. Plotting is isolated to a single, compact, device-dependent module to accommodate the wide variety of plotters in use. The highly modular system is written in IBM 360 assembler language and runs in less than 100K bytes of core. Its data base is a list-structured set of cells manipulated in virtual memory of a multipurpose file program. Addition of special features and alternative simulation algorithms requires little or no change to existing modules. For example, only a few minor changes were necessary when we decided, late in development of the system, to add flowchart drawing capability.

Status: The program began in 1968 and the system is in use but further applied research and application development are on-going. The software package has been debugged with documentation.

Hardware/Software:	Computer (BM S/360) Display Console (2250-1)
Publications:	H. R. Howie and R. M. Tavan, "OLLS: The On-Line Logical Simulation System," Design Automation Workshop Atlantic City, N.J. (1971).

PRINTED WIRING BOARD NUMERICAL DATA BASE VERIFICATION

C. R. Borgman
Sandia Laboratories

Objective: To provide a syntax check of Gerber codes defining a printed circuit board and to provide an indicator of the location and type of error encountered and, to provide a fast, economical visual check of the actual plots that will be generated on the Gerber photoplotters.

Scope: The system allows the input data to be on either punched cards or on magnetic tape. The program named "PEEK" and its associated program "REPEEK", which it automatically calls, operate on a NOVA 800 computer with 32K of core, a card reader, a magtape drive, a disk, and a line printer. These programs execute under DOS and are designed to interactively query and instruct the user to provide all necessary information to the program without prior knowledge of its operation procedure. The input Gerber codes must conform to the standard format for defining a two-sided printed wiring board in use at Sandia Laboratories, Albuquerque. A listing of the input on the line printer is optional. Error messages will appear in the listing with a pointer to the character in question if the listing option is selected and also will appear on the DVST. A hard copying device is attached to the TEK 4010 DVST to allow a copy to be made of all pertinent information. The program generates an intermediate data structure which is sorted on the disk attached to the NOVA 800. Since the final plots are generated from this file, the user may replot the plots without reentering his input data.

Methodology: The user places his input data (either a card deck or a magtape) on the appropriate input device. He causes the program PEEK to be executed in the NOVA 800 by using standard DOS command strings. He responds to the questions and commands which appear on the screen of the DVST. The desired results will be a listing of the Gerber codes and error messages if any, a plot of the lands, common circuitry and side 1 circuitry, and a plot of the lands, common circuitry and side 2 circuitry.

Status: The system has been debugged with documentation and is in operation.

Hardware/Software: Minicomputer (Nova 800)
Plotter 10
Terminal (Tektronix-4010)
Disk Operating System (DOS)
FORTRAN IV

OPTICAL PROCESSING TECHNIQUE FOR IDENTIFYING CIRCUITS (OPTIC)

William C. Burd
Sandia Laboratories

Study funded by Atomic Energy Commission

Objective: A geometric model of a printed circuit board by reducing data collected while scanning a colored design layout.

Scope: Plotting codes are generated from the model and used to produce artwork masks for etching and NC data for drilling. This process eliminates manual digitizing of the design layouts and thus realizes savings in manhours and equipment.

Methodology: Design layouts defining printed circuit boards originate in drafting organizations. They are regular line drawings normally made on grids. Color coding is used to separate the circuit's two sides. Average scanning time is 5-10 minutes. Several pattern recognition techniques are used in transforming scanner data into the geometric model. The boundary pairs are first reduced to contours complete with topology. Centerline segments are next extracted from the line contours. The total interconnects are formed from combinations of these segments. Component pin locations are entered using the Sandia Artwork Language (SAL) or by scanning dots and numbers. The number contours are recognized by considering Fourier shape coefficients and used to associate size information with the pin positions. The model is finally subjected to analytical clearance checking and automatically adjusted where necessary. Verification is performed on the DAVINCI interactive graphics system. Final artwork is generated on a Gerber precision plotter.

Status: The system is in use.

Hardware/Software: Computer (Nova 800, CDC 6600)
Color detecting high precision scanner
FORTRAN
Nova assembly language

SANDIA ARTWORK LANGUAGE (SAL)

William C. Burd
Sandia Laboratories

Objective: To facilitate rapid conversion of artwork specifications into plotting codes for Gerber Automatic Drafting Machines.

Scope: The language is an operator precedence grammar allowing powerful calculation capabilities. Jobs may be run either from remote time-sharing teletypes or by normal batch methods. Output media include listings, punched paper tape, card decks and magnetic tape.

Methodology: In addition to commands that produce a one-to-one correspondence in plot codes, SAL has matrix commands and pattern capabilities. Patterns may be built from commands (including previously defined patterns) and used in combinations of translations and rotations, thus taking advantage of the regularity of many artwork features. SAL's grammar includes conditional and unconditional branching, thus allowing looping and interactive calculations. The data structure (GERBER Codes) generated by postprocessing SAL can serve as an input to the DAVINCI system, thereby, providing an interactive graphics editing system.

Status: The system is in use.

Hardware/Software: Computers (PDP-10, CDC-6600)
FORTRAN

Publications: "Sandia Artwork Language (SAL)," SC-M-72-0155, March, 1972.

SANDIA IMAGE DIGITIZER, CONNECTOR, ANALYZER AND PLOTTER (SID CAP)

C. R. Borgman
Sandia Laboratories

Objective: A quick flexible mode of digitizing patterns and inputting these data into a computer. The connector, analyzer and plotter (CAP) is to develop computer techniques to process these data to determine information about the pattern.

Scope: The latest version of SID, SID-9, is an automatic "Image Digitizer" capable of digitizing any picture, object, scene upon which a closed circuit television camera can be focused. It has an adjustable level detector, which provides a two-level output (either on or off) of the input scene and the capability o- displaying this two-level digital picture on a TV monitor and of sending these data to a computer in a specialized format that conserves the amount of memory necessary to store the digital image.

Methodology: SID-9 has a resolution of 1000 x 1000. It was designed to use standard, commercially available parts. It uses a standard high-resolution closed-circuit TV camera as its input device and state-of-the-art integrated circuits, memories, and power supplies. SID-9 data are input to PDP-9 computer through its data channel. These data can be processed in the PDP-9 or output to any I/O device for later input to other computers. Once common mode of operation is to output the data onto seven-track magtape and send this tape to the central computer center for further processing. Other software options include the display of the digitized data on an interactive graphics display terminal attached to the PDP-9 for visual verification of the data. The data format stores transitions from white to black and vice versa.

Status: The system is in use.

Hardware/Software:
Computer (PDP-9)
Operating System (PDP-9 V5A)
TTL integrated circuits (SSI & MSI)
MECL integrated circuits
Memory (Cogar)
Closed-circuit high-resolution TV camera
Monitor

DELETE ADD VERIFY INTEGRATE NETWORK CIRCUIT IMAGES (DAVINCI)

William C. Burd
Sandia Laboratories

Objective: Printed circuit artwork edited in a graphic mode.

Scope: The input file consists of Gerber plotting codes, Sandia Artwork Language (SAL) programs, or data collected by scanning a colored design layout (Project OPTIC). The output contains plotting codes suitable for generating the updated artwork on a Gerber Automatic Drafting Machine and N/C information for drilling.

Methodology: Basic DAVINCI options selected by a lightpen allow the user to display various combinations of circuit layers. The pictures can be enlarged by a software window option to examine areas in closer detail. Clearance for electrical standoff is an important design parameter and the system provides several visual and analytic checking methods. Some automatic adjustment is available with the analytic checks. Manipulation capabilities allow parts to be added, deleted, revised or duplicated. Several methods for adding interconnects are provided to meet various requirements. In addition, a pattern option allows several items to be grouped together and revised or duplicated as an entity. Commands are oriented toward PC boards; produces masks, assembly drawings; and does clearance checks.

Status: The initial varsion fo the system is in use. A second improved version is in development.

Hardware/Software: Computer (CDC-6600, PDP-9)
Display (Vector General)
Operating system (Scope 3.3)
Sandia Interactive Graphics System (SICS)
FORTRAN

GRAPHIC AID FORINVESTIGATING NETWORKS (GAIN)

Dan Blazek
Sandia Laboratories

Objective: Application development to provide the capability to define circuit topologies in schematic format through an interactive display system and postprocess these circuit descriptions into card images suitable for input to the SCEPTRE circuit analysis program.

Scope: This application program provides the user with the capability to define the basic input descriptions required by the SCEPTRE circuit analysis program through the interactive cathode ray tube display system. Included in these input descriptions are circuit topologies, model topologies, element values or types, analysis outputs, and modes of analysis. Output from the analysis program is also displayed on the CRT in graphical and tabulated formats.

Methodology: Interaction with the CRT system is through a lightpen and keyboard assoicated with each terminal. In defining circuit topologies, the lightpen is used to identify node locations and the nodes between which circuit elements are connected. The keyboard is used to identify element values or device types as they are added to the display schematic. When the circuit topology has been defined, the user may add additional information required by the circuit analysis program. The lightpen is used to identify circuit elements for which output information is desired. The keyboard is used to add elapsed circuit time if a transient analysis is requested. After this phase of definition; the SCEPTRE input card images generated from the circuit topology and added information are displayed on the CRT. At this point, the user has the option of adding, deleting, or replacing cards through the CRT keyboard. After SCEPTRE execution (which is initiated through the CRT terminal), output results are displayed on the CRT. For transient analyses, plots of current or voltage versus time may be viewed sequentially. For initial condition analyses, the requested outputs are displayed in tabulated format. Tabulated numerical data on transient analyses are also available to the user requiring detailed information.

Status: GAIN is available to users through four interactive graphics terminals at Sandia.

Hardware/Software: Computers (DEC PDP-9, CDC 6000)
Cathode ray tube (Vector general)
FORTRAN
Sandia interactive graphics system software

Publications: "GAIN - An Interactive Graphics Interface for Circuit Analysis Programs," Sandia Devleopment Report SAL-73-0670, 1973.

APPENDIX B

Examples of CAD in Operation

Sandia Laboratories

Naval Electronics Laboratory Center

Charles Stark Draper Laboratories

Army Electronics Command

National Security Agency

Martin - Orlando

Harris Semiconductor

Sandia Laboratories

Date: 11-12 August 1975

Principal Contact: Dan R. Blazek
Sandia Laboratories
Organization 9624
Albuquerque, NM 87115
(505) 264-6141

Entrance requires an I.D. with photograph. Send clearance if possible--not absolutely required.

Summary: Four groups were visited.

1. P.C. and Drafting (Gino Carli, Dan's boss)
2. Hybrids
3. Integrated Circuits
4. Computer Aided Design & Analysis (Dr. Charles W. Gwyn) (505) 264-5373)

Software Packages. Sandia has several somewhat similar graphics systems for CAD.

GAIN - This is an interactive program which inputs a schematic in nodes and branches into the CDC 6600 through a Vector General CRT and an 18-bit PDP-9 minicomputer. Sandia has a pool of 3 CDC 6600's all working from one I/O queue. Only one 6600 handles graphics so that a GAIN user must "ring" the 6600 oeprator to insure that he gets the right machine. 20 second pauses for 6600 access are common using GAIN. The code is in FORTRAN and is 3" thick in printout form. Dan will send code if we furnish a magnetic tape. He uses the 6600 update package to generate mag tapes. GAIN outputs card images ready for SCEPTRE and lets the user Edit the output if he wants to change parameters. Once SCEPTRE has executed, the output is available on the Vector General as plots.

DAVINCI - This is a program, oriented toward PC boards, to layout and produce masks for photoprocessing. It also uses the Vector General, PDP 9, and CDC 6600. IGDS-5 will do most of what DAVINCI will. DAVINCI provides a "clearance check" which allows one to expand lines to look for problems.

MASK - This program was purchased from Systems, Science and Software (10 October 1971), now Computervision of La Jolla. In capability is also looks a lot like M & S systems.

All of these programs generate data fields in CDC 6600 for Gerbers 2033, 1232 and Xynetics 1100 plotters. The Precision Graphics group also has a PDP 9 remote unit to the 6600. They read the file to magnetic tape and transfer to the plotters.

IC layout is done by Chuck Gwyn's group. They use Auburn's CAD package and say it works well, better than NASA's BOOLEAN. Palmer at Los Alamos also uses it. Chuck uses SALOGS, a logic simulator, and PR2D, and RCA layout program. Sandia has optimized routing and improved execution time (20 to 1 in some cases) over the RCA version. Chuck has a PDP 15 remote to the CDC 6600 for his work. He is setting up a new IC facility that will be a whole building full of equipment to begin operation in Feburary 1976. He would be a good contact for Bill Carroll. He knows John Gould. He suggests Hightower at Bell Labs as being a routing expert.

The hybrids group at Sandia does all their work by hand. In fact, Bendix, Kansas City, does most of their construction. Sandia engineers spend weeks at a time in Kansas City redesigning and testing the hybrids. There is talk of closing down the hybrid group at Sandia.

Computing Hardware at Sandia

Large Machines: 3 CDC 6600's
1 UNIVAC 1108
4460/4020 Stromberg Carlson

Remote Terminals: 2 PDP9's at Blazeks
1 PDP9 at Precision Graphics
1 PDP15 at Chuck's group
CDC Sys 17's (Disc, CDU, High Speed CR and LP)
2000 Series (MICOM)

Each PDP 9 has CPU (18 bit), 512K word FHD, PTR/P, 2 Dectapes, magnetic tape (7 track), Vector General Graphics Unit ($60,000), Tektronics 4014, 24K x 18 bit core memory.

The Gerber plotters are driven by HP2116's. The Xynetics 1100 uses a lockheed MAC/JR mini, and a magnetic tape unit. The Xynetics use magnetics to move pen and it is very fast.

Sandia is just purchasing a new Applicon AGS/700 System. The applicon has 3 terminals (4014 with tablet, a 14.5M word disk (2.5M words is used by system software, PDP 11/35 CPU, magnetic tape, 2 dec-writers, and a digitizer/plotter). Commands are entered by pattern recognition on the tablet. Write to:

Applicon, Inc.
154 Middlesex Turnpike
Burlington, MA 01803
(617) 272-7070

The AGS/700 costs about $200,000. It sorts 4014 commands to minimize CRT drawing time. It has 16 levels, with 3 remove-bins, for an effective 64 levels.

Naval Electronics Laboratory Center

Date: 13 August 1975

Primary Contact: Dr. Dean McKee, Code 4800
Naval Electronics Laboratory Center
271 Catalina Blvd. (Point Loma)
San Diego, CA 92152
(714) 225-6877
Autovon 8-993-6877

Dean is a ceramics engineer who came from industry to the Navy in 1973. He's from Michigan or Illinois and has liven in L.A. Age: ≈ 50 (has a 26 year old son). Dean met Vic Ruwe at a conference and had Sal Cruso MSFC for a visit on 28 July 1975.

Summary:

Organization. Microelectronics at NELC is currently divided between the Electronic Materials Science Division and the Microelectornics Division (O.H. Lindberg). The Microelectronics Division is further divided into 3 groups.

1. An advanced devleopment group (Issac Langnado) that makes wafers using metal gate CMOS technology; they are developing a silicon gate capability; a new ion implanter ($150,000) is just being installed. One current project of this group is an integrated optics light detector and amplifier being built by IBM Federal Systems Division, maybe in Huntsville. This group builds chips for use by the hybrids group. Another current project is a CMOS ROM chip 256 x 8 to be placed in a hybrid package 4K x 8.

2. The LSI and circuit design group (Gene Haviland) does most of the electrical design and chip testing. They have a Fairchild

Sentry 600 LSI tester ($200,000) which is available from:

Computervision
201 Burlington Road
Bedford, MA 01730

3. The hybrids group (Dr. Dean McKee) fabricate other people's designs. They get support from the LSI group and from users when circuit design problems arise. They are funded by Navy Industrial Funds so they must find customers. The hybrids group has produced 20 or so different jobs. Several are very complex, 1.5" x 2" and more compact than the Jennings job. The group is in a lull now with only 5 people. They have done several digital CMOS projects and some analog video work. They sometimes use thin film on hybrids. They buy alumina substrates coated with nichrome nichol gold. Dean says it's easier to go dense in one layer, and it can be as cheap or cheaper than thick film. He took issue on this point with Jerry Sargent, USF, at a recent meeting.

Mission. NELC advises Navy at all levels on μ-electronics. They are chartered to do prototype development and advanced R & D.

Consultant. Al Tuszyrski
Electrical Engineer
University of Minnesota
Minneapolis, MN 55455
(612) 373-2970

He comes summers and other times during the year.

Charles Stark Draper Laboratory, Inc.

Date: September 9, 1975

Contact: Richard M. Tavan (617) 258-1469
Cambridge, MA 75 Cambridge Parkway

CSDL has two computer systems on which CAD is done. An IBM 360 is used with the On-Line Logical Simulation (OLLS) System while a DEC PDP 11/40 is used with some Tektronix graphics terminals, storage slave screens, an Interact IV plotter/digitizer, and peripheral storage devices for a graphics system.

The OLLS system was developed by CSDL for NASA to provide fast, precise system documentation and accurate logic simulation to improve the design process. With this system a designer an interactively design layout and simulate large digital systems through the IBM 2250 CRT. Or, if terminal time is of concern, information can be inputted through a card reader and, within the limitation of a lineprinter, outputted. This feature is especially nice for off-line data modification. The logic simulation completely simulates each device behavior and standard Boolean forms whose variables are the terminal names used in device definition. Time delays for the devices can be designated using a simple syntax. Using a schematic data base, the logic simulation program runs in a 120K byte partition in a batch mode. Although the software has been highly modularized it is written in IBM 360 assembler language so that it would have to be completely rewritten to run on our CDC 6600. Therefore, it would not be cost effective to implement on our computer system.

CSDL has developed a DEC PDP 11/40 based interactive graphics system for drawing mechanical systems and electrical networks. This

development was funded by a 1972 Fiat contract. The basic software package with which CSDL started was the same one Gerber Scientific Instruments started with. Gerber developed a three dimensional design system whereas Fiat and CSDL developed a system to do mechanical design and documentation. The CSDL system runs in batch mode under a DEC (DOS 11) operating system. The program is written largely in FORTRAN IV with some macro assembler interfaces for I/O, etc. The code meets ISO (European) and most ANSI (American) standards for FORTRAN programs.

The chief advantage of this system, according to Tavan, over the M & S Computing type, is the use of a geometric construction approach rather than a connect the dots approach. The current version of the mechanical design program was completed in December of 1974. In order to make the program useful for printed circuit board layouts and design the program had to be adapted. The first phase of adaptation, begun in January of 1975), was completed last June and allows CSDL to design multilayer boards for Trident. The hybrids and IC groups will eventually use the system. There are several output programs so that data out is available for most photoplotters. The hardware complement includes a DEC PDP 11/40 with 24K words of core, EIS and FIS, a Computervision Interact IV digitizer/plotter, Tektronix 4010, 401w, and 4014's, a Plotter LP3000 printer, two RK05 disks and two Dectapes. The hardware belongs to Fiat. Draper is buying their own set of hardware centered around DEC PDP 11/45's and RSX11/M operating systems.

CSDL designs their own small or complex p.c. boards. CSDL has used Algorex to design their medium sized p.c. boards. (Since Algorex's automated system can't handle large, complex boards, they are done in-house.)

U.S. Army Electronics Command

Date: 10 September 1975

Contact: Randy Reitmeyer
Ft. Monmouth, NJ

General

The integrated circuits group at ECOM is divided into linear and digital sections, each containing 4 engineers/designers plus a technician. There is a separate hybrids group which we did not visit. Randy Reitmeyer has an Applicon system upon which he does most of his designs. They are heavily involved with RCA-Camden. Reitmeyer reports to Dr. Clare Thorton who is the LSI expert at ECOM. Another group headed by Bob Larken has about $6 million in computer graphics equipment and is connected on the ARPA network. The Applicon system was purchased as an "interim" measure and Reitmeyer expects to use Larkins locally developed system in the future.

LSI Placement and Routing

ECOM has funded several years work at RCA-Camden. The original PRF (place, route, and fold) program used single entrance standard cells, that is, cells with entrance only on one side. Several versions of this program have since evolved. John Gould (NASA) developed with RCA-Camden the PR2D (placement and routing in two dimensions) and Chuck Gwyn of Sandia Laboratories has developed his own independent version. ECOM currently is expanding its version to MP2D (multipart two dimensional) placement and routing; again with RCA-Camden. Features are double-entry cells with feed through cells having dummy contacts on two sides. These

features have great impact on density. The goal of this new ECOM version is automation of high density circuits. Normally high density is obtained by custom LSI circuits whereas ECOM wants high density using standard cells. ECOM wants to minimize the area per active device ratio. The MP2D automatic system is now approaching hand designs. The RCA-Camden contact is Al Feller. The program is owned by the U.S. Government and runs on an IBM 360/65. The execution time is 30 min. to 1 hour for circuit complexities of 500 gates/chip. ECOM will make this program available to MICOM when it is finished. Modifications to MP2D are Sub-chips (large standard cells) and a Common Data Base for logic simulation, test generation, and previous versions of the program. The first will be done next year and the latter began in July. ECOM plans a big project to develop a new set of standard cells for SOS (silicon on sapphire).

ARPA Project

Dave Kennedy and Fred Lindholm, University of Florida, and Jim Meindal, Stanform University, are participating in a $500,000, 15 month project for ARPA on LSI technology and automation. The project is an outgrowth of a 1 year study contract by Kennedy. A request for the study report should be made to Kennedy. In the new project Kennedy is attacking device modelling aimed at automation using Monte Carlo techniques. Stanford University is investigating processes. Sandia was to do automation of placement routing, etc., but this part was cancelled. Dr. Clare Thorton is on the ARPA steering committee for this project. He did handle microelectronics at Philco-Ford before they closed this division.

Other CAD Programs

ECOM uses several other CAD programs.

MSINK - MOS modelling program

SPICE - bipolar circuit analysis

FILTER - filter design program for an Op amp design

RFAMP - IF/RF amplifier design program with impedance matching, etc.

COD - constrained optimal design, a general optimal design program

SUPER-SCEPTRE
ECAP
PANE
CIRCUS — circuit analysis programs in FORTRAN

PCBOARD - a pc board layout program being developed in house

To get these programs, Bob Sutton in Stanford microelectronics group has MSINK and SPICE; Randy Reitmeyer, FILTER and RFAMP; and Bob Larkin, COD, SUPER-SCEPTRE, ECAP, PANE, CIRCUS, and the new PCBOARD program.

Equipment

The APPLICON AGS700 system is composed of PDP 11/05 with 24K core words, DEC 9 track magnetic tape, 36 megabyte DIVA disc, 256K fixed-head disc, FACIT paper tape punch, dual cassette magnetic tape, Tektronics 611 with hard copy, Alphanumeric display with keyboard, Calcomp 563 drum plotter, and Tabletizer digitizer and editing station. They have no flatbed plotter. They use RCA TCC040 system for special custom IC's (PMOS and CMOS). They use a stand DOS MOS Universal Array Metal Pattern.

A Gyrex Pattern generator 1001-4 can produce 3" x 3" glass plates to .1 mil accuracy. To generate a plate for 168 gates for a 188 x 188 mil area takes 4 hours. The wafers are partially processed by RCA and ECOM designs the custom layers. A two month turn around is typical. PC boards are done by 2 technicians who layout about 200 boards per year. This group at ECOM serves as a service bureau for the other ECOM laboratories.

National Security Agency

Date: September 11, 1975

Contact: Paul Losleben (301) 688-7815, Autovon 235-7815

General

NSA has been developing a set of computer aided design programs for the design of LSI circuits. Westinghouse (at Friendship Airport) is responsible for making these programs available on the GE Mark III Computer Utility. The Westinghouse contact is Jon Squire (765-6368). NSA data processing is usually done on dual Honeywell 6050 processors in the batch mode.

Acquisition Procedure

NSA plans to use Westinghouse as the distribution center for this CAD package. Access should be requested from Paul Losleben. NSA then must authorize Westinghouse to provide documentation and open the GE Mark III files to a user. Two options will be available. First, a user can rent time on the GE system and access the system by remote terminals. Second, one may obtain source listings of the programs (20 programs and 250,000 cards) and try to run them on their own machines. Only the GE version will be maintained. Most of the code is in FORTRAN. Paul will supply documentation directly on cell families that he uses. Note that NSA will place limits on the use of the programs, for example NO FOREIGN.

Current Status

The cell level and Logic simulation portions are running now; the layout and other small programs will be ready in October.

Other Contacts

Paul recommended several other people who are active in this area.

1. Steve Szygenda, Comprehensive Computing Systems, Austin, Texas. Steve developed TGAS at SMU. It is installed on CYBERNET and runs on CDC equipment.
2. John Fike, SMU
3. Mike Heims, Harris Semiconductor
4. Mel Breuer, Southern Cal
5. Al Korenjak, RCA Laboratories, Princeton (609-452-2700)
6. Bruce MIddlesworth (688-7483), NSA, is working on a PC board program in machine code on the H6050.

Placement, Routing Problem

Several companies are active in the placement and routing areas. Redac does automatic layout and placement for single, double, and multi-layer boards. Scientific calculations provides similar capabilities. Algorex is another, but they only sell service. The really successful routing programs are for fixed geometries. Usually the net interconnection is the only concern. For analog routing a general, variable-geometry router is needed and the line length, coupling, capacitance, etc., effects must also be examined.

Production Facilities

NSA is now installing an IC facility for prototyping work and for highly classified projects. They currently contract most of their work to Harris-Melbourne, TRW-Redondo Beach, and RCA-Camden. RCA uses their own automation package. Previously NSA has contracted with Collins, TI, Motorolla, and Solid State Scientific.

Graphics Facilities

NSA uses a Computervision graphics system for schematics and physical layouts. The system has some cross check features to ensure correspondence between schematics and physical layouts, such as the same number of transistors. NSA describes each device in algebraic equations with parameters being the length and width. Thus the physical size and electrical properties are available for check programs.

Cell/Circuit Design System

The NSA computer aided design system consist of a cell/circuit level and a chip/logic level, as shown in the accompanying diagrams. The purpose and function of each routine is summarized below:

ARTCELL - This program traces schematics and performs complex schematic-layout cross checks. No auto-layout is used for cell generation; devices are layed out at 1000X on grid milar. ARTCELL has been used by Westinghouse to layout hybrids. It has no restrictions on wiring channels and uses only orthogonal geometries, i.e. no diagonals or curvelinears are allowed. ARTCELL performs design rule, net, and capacitance checking. It takes about 30 minutes for a 100 component circuit on the H6050. ARTCELL has overlayed code and data structures with two assembly bit manipulation routines.

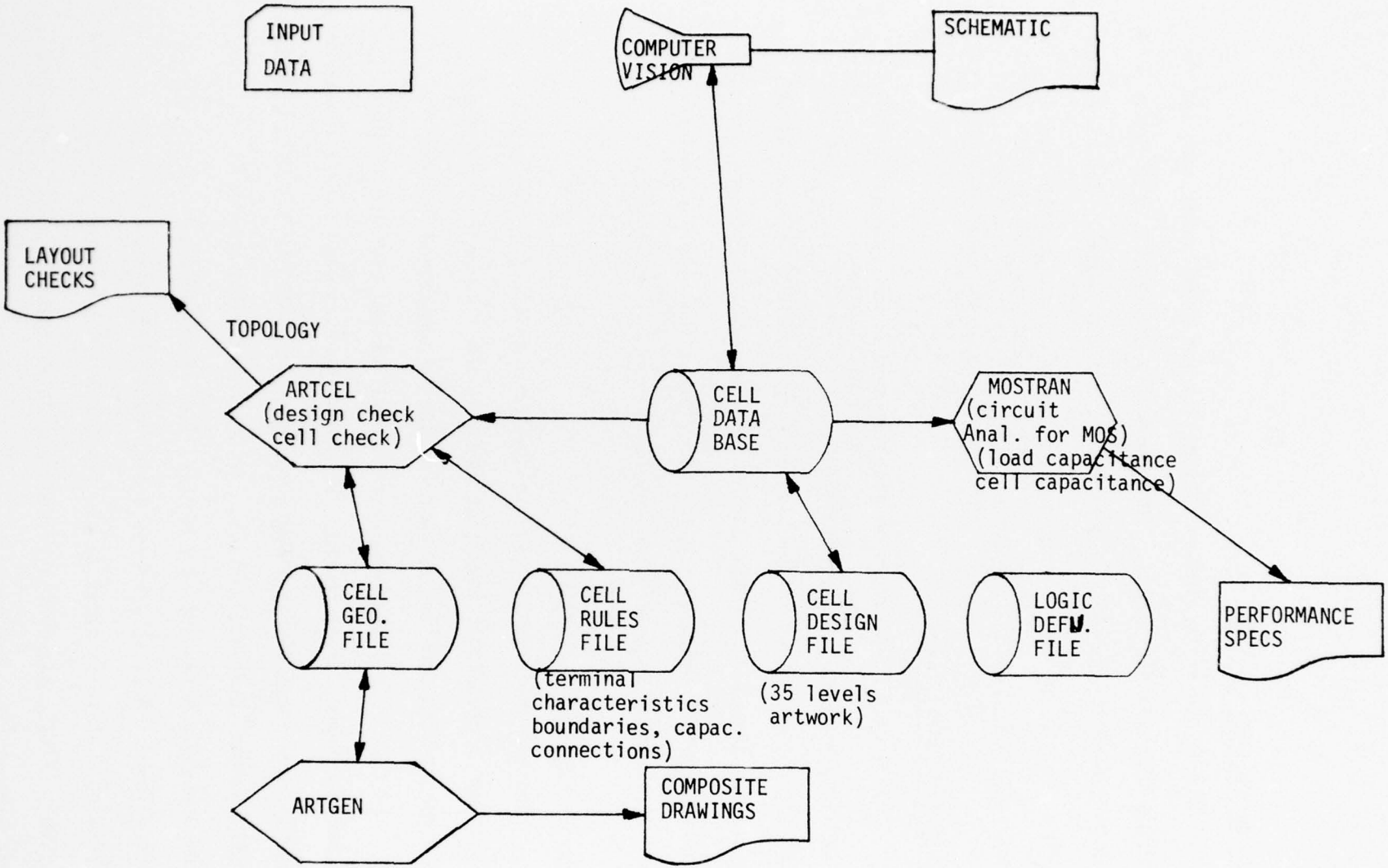

Figure B-1. Cell/Circuit Design System

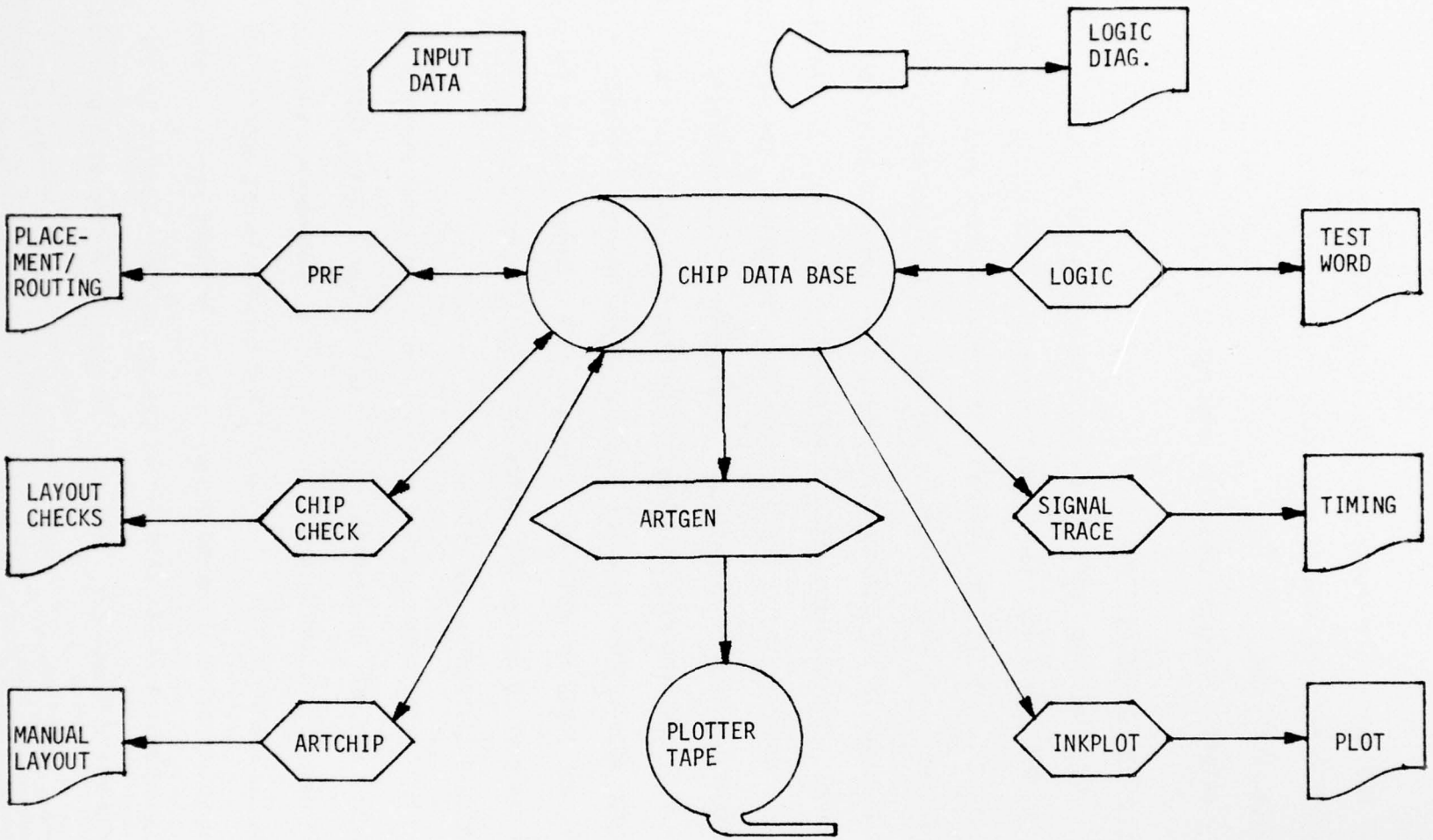

Figure B-2. Chip/Logic Design System

MOSTRAN - This program performs circuit analysis for MOS. It is different from the MOSTRAN available in industry. It does work like ISPICE, ECAP, etc.

ARTGEN - produces composite drawings of cells.

Chip/Logic Design System

The chip/logic design level has a number of CAD routines.

LOGIC - This is a logic simulator written in a special language which is translated into FORTRAN. It uses simulation word and bit variables, works with testwords, and uses the D-algorithm with heuristies and a random number generator. It only generates good tests for small circuits. Testword completeness verification is extensive. The program lists undetected faults and does some fault isolation. The major emphasis in LOGIC has been on generality. It has been used successfully on MOS, TTL, ECL, and some A/D interfaces. The major defect is run time. The program does not use parallel techniques now, however a version is now being developed for delivery in January 1976. Normally LOGIC is used by the designer to design and verify his circuit/testword set before he continues his design for silicon.

PRF - This program is an outgrowth of the original Banning program. Don Durr who did the original work at RCA is now at NSA. Collins (Cal), NASA-Huntsville, and Motorolla have standard cell programs which came from Don's work at RCA. The current NSA version is 3rd generation. It uses an iterative placement scheme to seven or eight levels. Using the NSA programs, a 22 LSI chip system (Vinson system) was done by one engineer and 5 designers took about 14 months. A chip with problems

could be redesigned in 2 weeks. The Vinson system has chip types: bit synchronizer, memory, word decoder, receiver controller, alarm tone generator, etc.

CHIP CHECK - This program is similar to ARTCELL at the chip level; it performs the same checks at chip levels. It is limited to 500 component complexities. It checks interconnect widths, etc. and does net checks with simplified interconnects.

ART CHIP (CHPCHP) - This program designs things which don't fit standard patterns. It is used to manually layout out in the BATCH environment. Could be done by interactive graphics (Computervision).

SIGNAL TRACE - This program checks timing of dynamic 2Ø logic; NSA doesn't promote this one. A new program will be ready next year.

INKPLOT - This routine gives at quick check at 100X, no cell detail is shown.

ARTGEN - This routine generates cell plots for Gerber 1000, 2000 interface and the ELECTROMASK DAVID MAMN 300 pattern generators.

Martin - Orlando

Date: 4 September 1975

Contact: Sam Bennett

CAD Programs in Use

Martin Orlando uses the design automation package developed by NASA's Marshall Space Flight Center. Programs packages include a Macrodata System for graphic layout, FETSIM for circuit analysis, and LASAR for array tests; EMAG is under procurement. They do custom CMOS work. They use SCI-CARD P.C. layout routine via terminal to an IBM 370.

Hardware

Macrodata MD170 System
- Interdata 4
- Caelus Disc - 2.4 Mbytes
- PerTec Mag Tape - 9 track
- *Tektronix 611*
- Computek CRT Terminal
- Calcomp Drum Plotter 563
- Macrodata Digitizer Board

Taradyne Automatic I.C. Tester
- System J261
- PDP 8/i
- *Magnetic Tape*
- Line Printer
- Tests 400 different device types

HP 9500D Analog Testing System
- Freq.: $1\text{-}10^9$ Hz
- Tests components

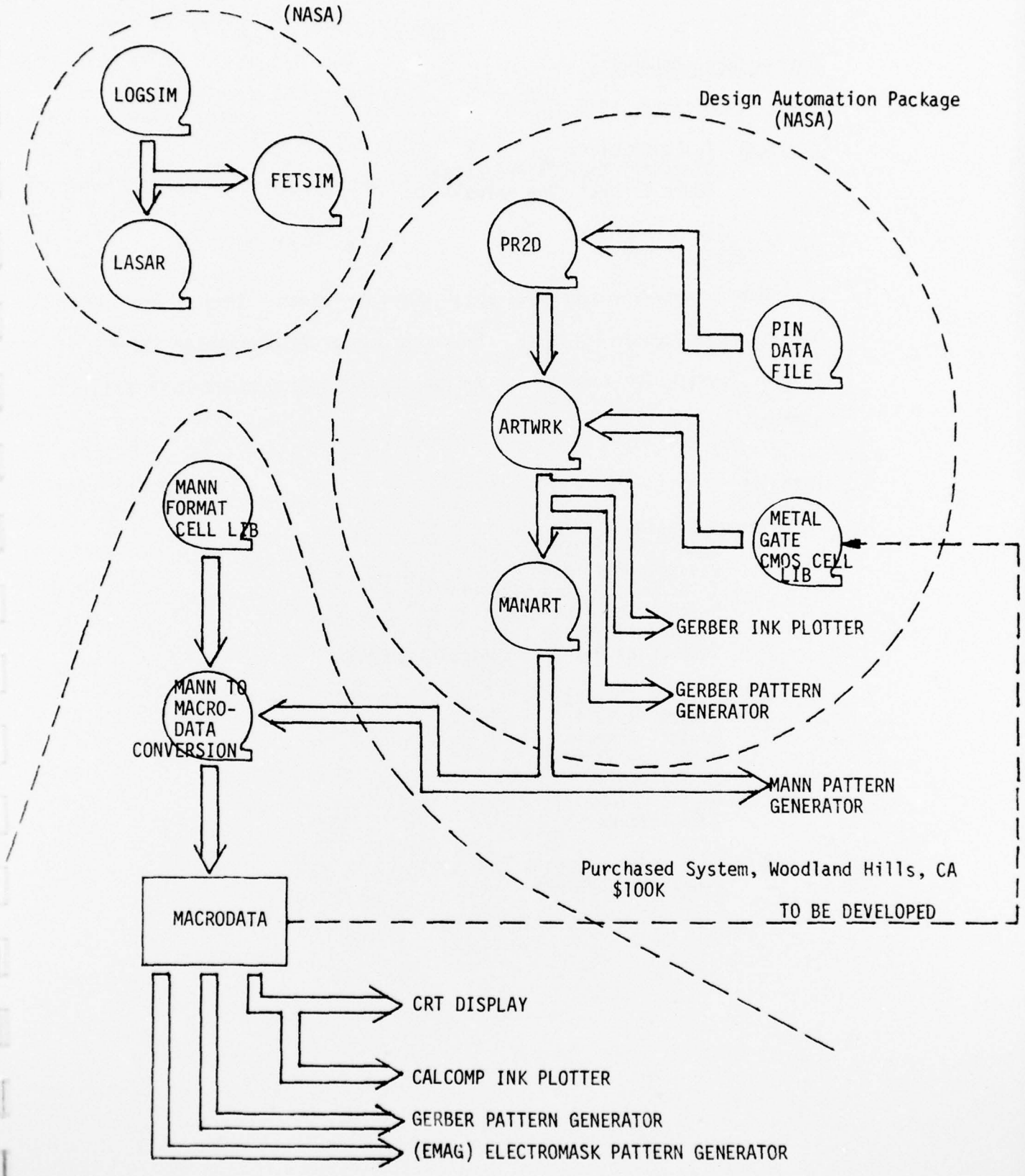
(NASA)
LOGSIM
FETSIM
LASAR
Design Automation Package
(NASA)
PR2D
PIN
DATA
FILE
ARTWRK
METAL
GATE
CMOS CELL
LIB
MANART
GERBER INK PLOTTER
GERBER PATTERN
GENERATOR
MANN
FORMAT
CELL LIB
MANN TO
MACRO-
DATA
CONVERSION
MANN PATTERN
GENERATOR
Purchased System, Woodland Hills, CA
$100K
MACRODATA
TO BE DEVELOPED
CRT DISPLAY
CALCOMP INK PLOTTER
GERBER PATTERN GENERATOR
(EMAG) ELECTROMASK PATTERN GENERATOR

Figure B-3.

Harris Semiconductor

Date: 5 September 1975

Contact: T. Lamar Clark
Director, Speical Products
(John Cornell, Bob Heins)

CAD Programs in Use

Harris was very secretive about their operation. They do use ISPICE and an NCSS computer terminal. They also use a CALMA computer aided graphics system for topological design, as well as an older Computervision system.

Hardware

Computervision System
- Data General Mini
- Cassette Mag Tape
- Info. Data System Disc
- 9-Track Mag Tape
- Digitizer/Plotter
- Tektronics 611 with speical keyboard

Calma System (newer)
- Tektronix 4014
- Speical Console
- Data General Mini
- 30 Mbyte Disc
- Magnetic Tape
- 2 Digitizers

Plotters, under Magnetic Tape Control
- 2 Calcomp plotters